BERT

FPGA based Bit-Error-Rate-Test for highspeed interfaces

- test for Gigabit interfaces
  - PCIe · USB 3.0 · SATA · Gigabit Ethernet
- for use in production and development
- validation of transmission lines
- visualisation of errors using eye diagrams
Technical specification & application

BERT — Bit-Error-Rate-Test

Adaptable
- flexible application potentials and easy adaptation to different stages of the production and development cycles

Extended Test Analysis
- visual presentation of transmission quality
- Evaluation and analysis of interface quality

Test From Inside
utilisation of onboard devices for testing
PCBs can be connected via their standard interfaces

ChipVORX-I/O module with test adapters for PCIe x8 plugin cards

Parameters | Data
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access technology | JTAG based control of FPGA embedded instruments
test methods | eye diagrams and Bit-Error-Rate-Test (BERT)
GBit channels per FPGA | only limited by utilised FPGA
different test settings | Peer-to-Peer tests or loopback tests – depending on used FPGAs and design
Multi-Link bus systems | supported via parallel instantiation and execution of BER-tests using all connections
interactive control of Tx/Rx parameters | FPGA properties can be adjusted dependent on parameters like on-the-fly controlled preamplification, voltage fluctuations and distortion - without design synthesis
test of GBit I/F with no onboard FPGA | possible by using external ChipVORX-I/O modules and utilisation of the targets loopback mode
software support | automatic program generation, integration into SYSTEM CASCON platform
supported GBit link protocols | PCIe (x1/x4/x8/x16), USB 3.0, SATA, Gigabit Ethernet

Made in Germany