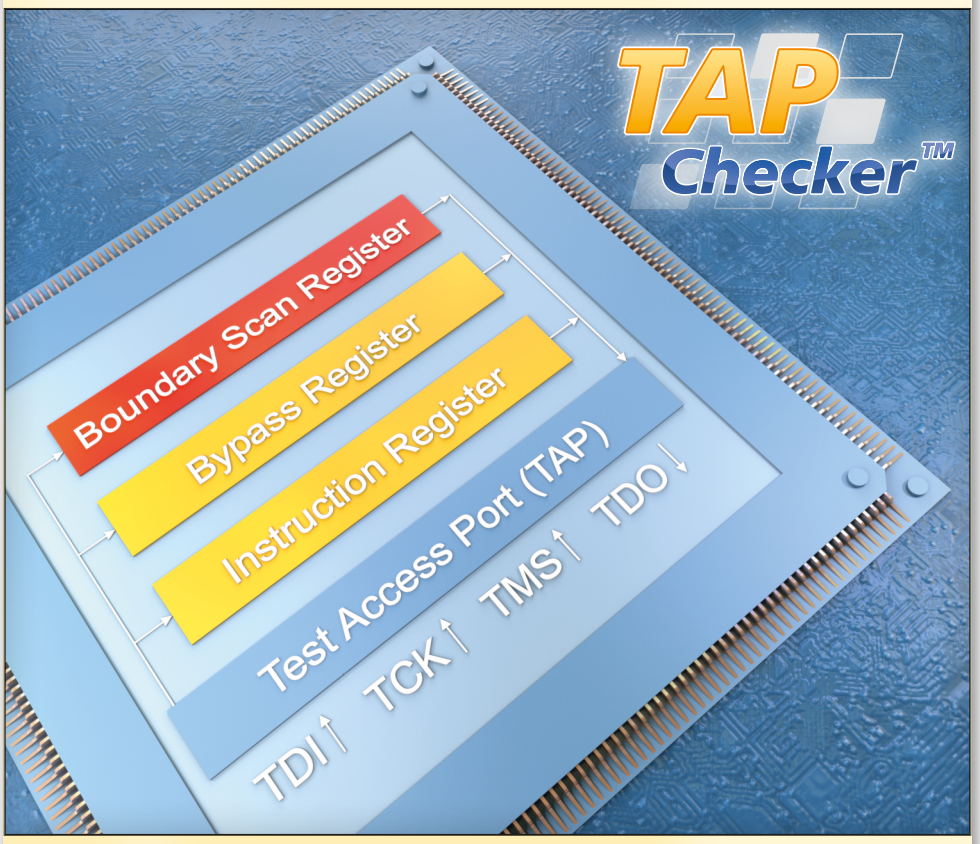
TAP Checker™

Product Information



- **Automated testbench generator for IEEE 1149.x ICs**
- **Full validation of Boundary Scan designs**
- **Extended functionality for multichip modules and 3D chips**
- **Compliant with all standard simulators**
- **Test pattern export to chip test systems in production**
- **Available for Windows, Oracle Solaris and Linux**

Boundary Scan (IEEE Std. 1149.x) is a revolutionary technology substituting physical access via nails and probes by means of special on-chip electronics (electronic nails) in conjunction with a dedicated four-wire bus. TAP Checker is a powerful EDA tool to validate such structures. Both the virtual verification based on functional simulations, and the physical test of the silicon by respective chip test systems are supported. TAP Checker can be utilised also for modern IC packages such as Multichip Modules (MCM) or 3D chips.

GOEPEL electronic

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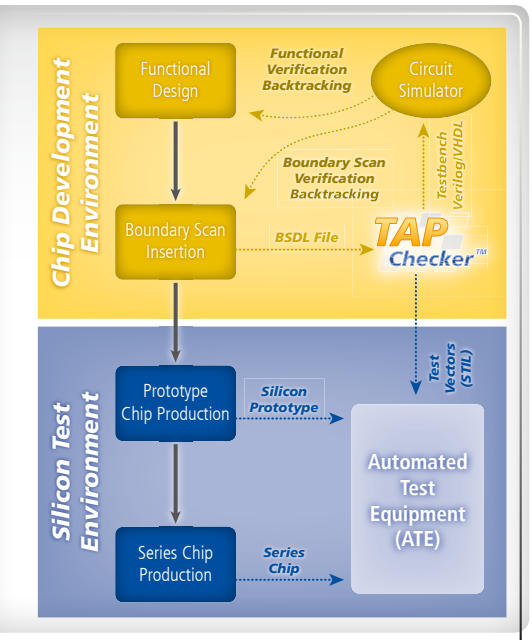
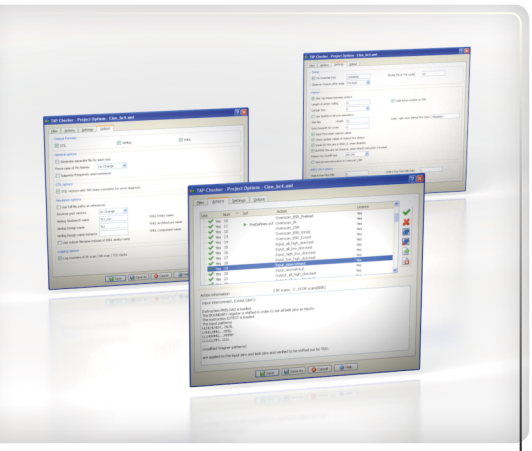
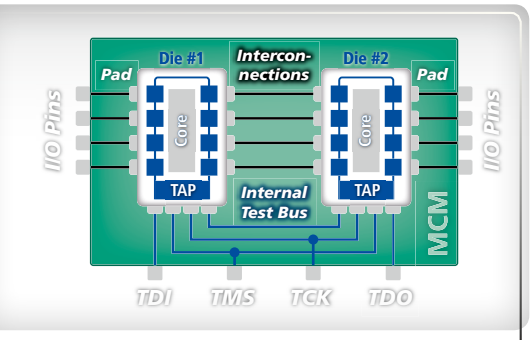
TAP Checker™



TAP Checker utilisation in the design and test workflow



TAP Checker graphical user interface (Windows)



TAP Checker also covers multichip modules

Automated Testbench Generation

Basically, in addition to the core logic's functional behaviour, required Boundary Scan features must be implemented and validated during the design of ICs with IEEE 1149.x characteristics. TAP Checker provides for minimising the number of verification iterations by the simulation of automatically generated test benches. The target's BSDL file works as an input, to be utilised for numerous procedures. These include:

- Syntax and semantics checks
- Generation of TAP tests
- Generation of register tests
- Generation of scan cell-to-pin interconnection tests
- Generation of special toggle tests
- Usage of customer-specific initialisation pattern
- Test of chained TAPs (multichip modules)
- Test of nets between dice (multichip modules)

In total, TAP Checker provides more than 70 different test options, and is able to support several Boundary Scan standards, which are:

- IEEE 1149.1 ("classic" Boundary Scan standard)
- IEEE 1149.6 (test of advanced interconnections)

Software control is executed dependent on the selected operating system per command line or GUI.

Connections to Simulators and ATE

TAP Checker supports virtual EDA environments as well as the validation of real silicon on a chip test system, wherefore several vector export options are available:

- Simulators: Verilog (IEEE 1364) / VHDL (IEEE 1076)
- Chip tester: STIL (IEEE 1450)

Additional interfaces are provided on request.

Supported Platforms and Order Information

TAP Checker can be run in all common operating systems Windows, Solaris and Linux with diverse licensing models. The standard packages can be upgraded through a number of extension options. GOEPEL electronic offers special services to support customer-specific Boundary Scan designs.

Product	Vektor-export	IEEE 1149.1	IEEE 1149.6	MCM support	Product number
TAP Checker Standard Edition	✓	✓			TCE-01x
TAP Checker Advanced Edition	✓	✓	✓	✓	TCE-03x

Additional information can be found at **goepel.com**.

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