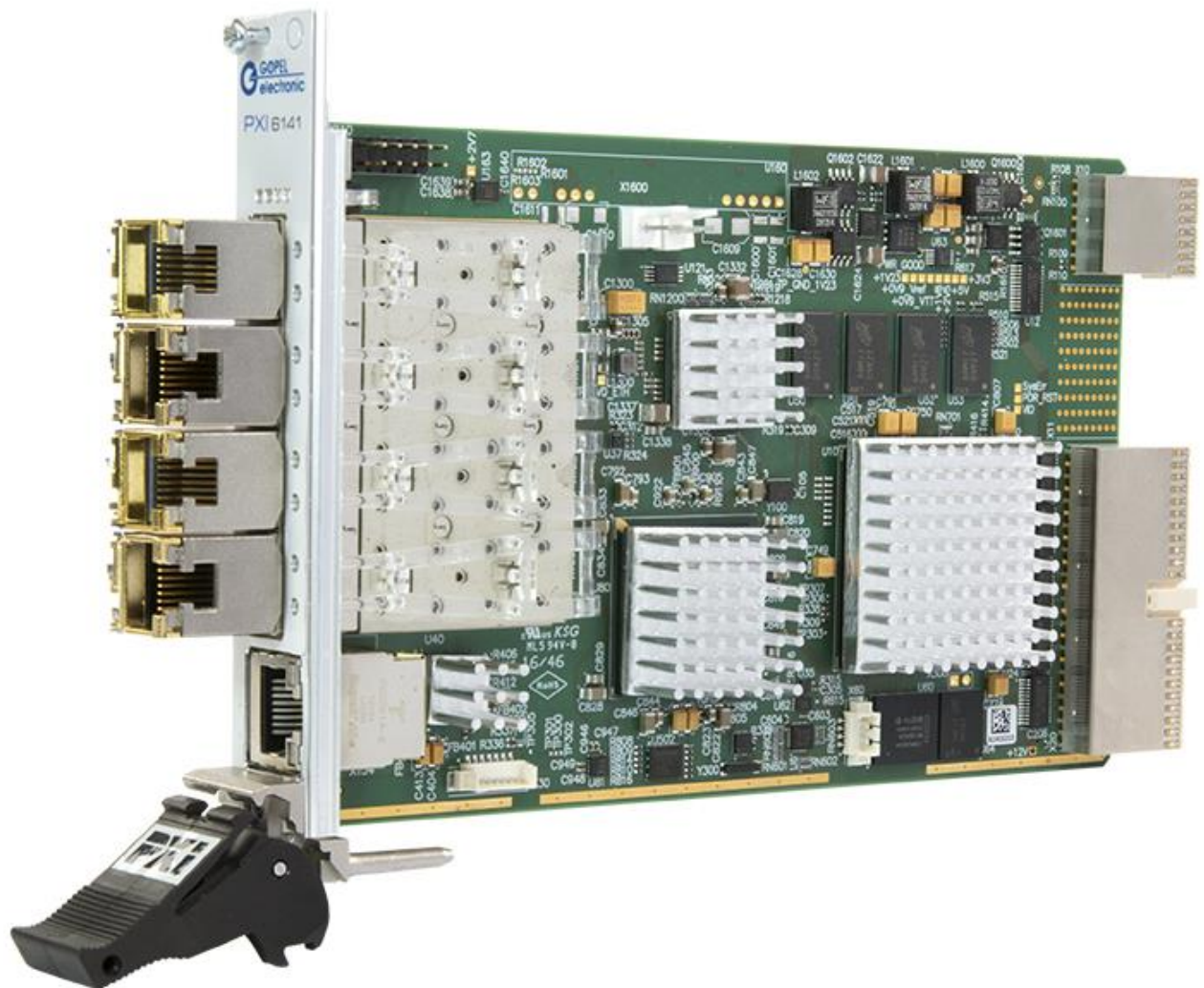# PXI 6141 (Ethernet Board)

User Manual (Translation of Original Docu)

Document Version 1.4

GOEPEL electronic

Enjoy Testing

1 Liability and Warranty Exclusion

The PXI 6141 controller board has not been developed, tested or intended for use in safety-related applications. Do not use the device for safety-related systems or vehicle subsystems. The use of such a device within motor vehicles to control the main vehicle functions can be dangerous and lead to malfunction of motor vehicles.

In no event shall **GÖPEL electronic** be responsible for any direct, indirect, incidental, special, exemplary, or consequential damages (including but not limited to the purchase of replacement goods or services, loss of use, loss of data or profit, breakdowns, injury, or potential death) in any way in the case of improper use of the PXI 6141 board.

2   Board Installation

2.1   Hardware Installation

Please make absolutely sure that all hardware installation work is carried out with your system switched off!
The power supply should be disconnected.

Please refer also to the User Manual of your PXI system for additional installation instructions that possibly have to be followed.

Electro Static Discharge (ESD) can harm your system and destroy electronic components. This can lead to irreparable damage on both the controller board and the system hosting the board as well as to unexpected malfunction of your test system.
Therefore do not touch the board surface or any connector pins and electronic components.

The **PXI™** system is to be opened according to its conditions. Select a free slot in your system. Remove the existing slot cover from the selected slot. To do this, unscrew the fixation screw(s) and remove the cover from the slot.

(If it is necessary to exchange transceiver modules,
pay attention to the general rules to avoid electro static discharging.
The modules can be plugged or unplugged under voltage; however, we recommend that you only replace the modules when they are switched off.
It is essential that the modules are inserted in the correct position.

Insert the board carefully into the prepared slot. For PXI boards, use the lever at the front plate in order to push in the board finally.

After contacting the board, it is fixed to the front panel with the screws. Now, the board has been installed correctly.

Afterwards, the operations that make the system functional again must be carried out.

2.2 Driver Installation

2.2.1 Windows Device Driver

PXI **6141** boards can run on Windows 7, 8 and 10.

Due to the plug-and-play capability of Windows, the hardware wizard automatically starts a driver installation for each newly detected hardware component.

The hardware wizard can carry out the installation of the device driver by using the *inf* file contained on the enclosed CD.

A restart of the system is not absolutely necessary.

After the hardware installation/driver installation you can check whether the boards have been properly integrated into the system:

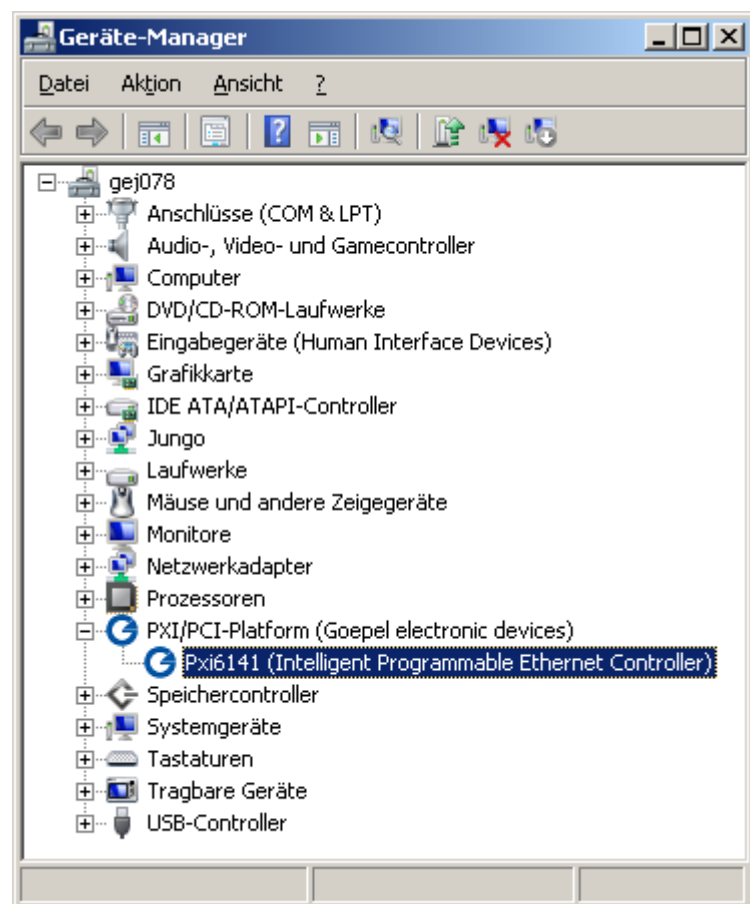Figure 2-1: Windows

2.2.2 Ethernet

If the Ethernet interface is used for communication with the control PC, no driver installation is required.

The device can be addressed directly via the **IP Address**.
This **IP Address** can be changed by the **HardwaremExplorer**.
The newly set **IP Address** becomes effective after a restart:
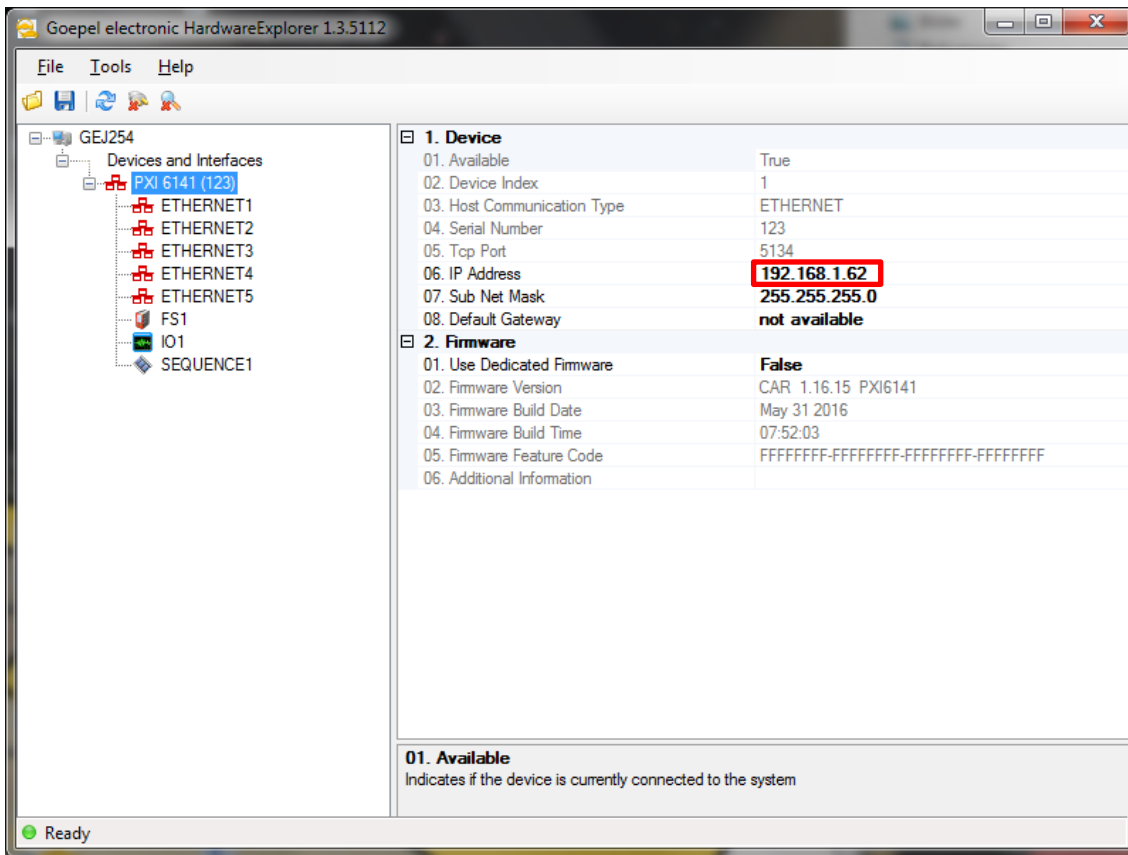
Figure 2-2: IP Address in the GÖPEL electronic HardwareExplorer

2.3   Notes on the Firmware

2.3.1   Firmware Update

In the course of technical progress it may become necessary from time to time to update your hardware with a new firmware version.
Proceed as follows:

- Download the current Firmware Update-File
  from *genesis.goepel.com*
- Open the GÖPEL electronic HardwareExplorer
- On "Card" (PXI6141) select "Flash Firmware"
  with the right mouse button
- On "Flash Firmware" select the Update-File
  with the left mouse button and execute it (e.g. by double clicking)
- When the progress bar is finished in the "Flashing..." window, press
  the "OK" button in the following "Success" window
  with the left mouse button

Please make sure to use the correct firmware version when updating the firmware.
Installation of an incorrect firmware version could lead to loss of functionality and thus cause malfunctions of your application.

In such a case, reinstalling the correct firmware level can restore functionality.

The interface options supported by the firmware are listed in the following table:

Software Interface	Hardware Interface (plug-in place)
Ethernet1	ETH0
Ethernet2	SFP0
Ethernet3	SFP1
Ethernet4	SFP2
Ethernet5	SFP3

ETH = Ethernet RJ45
SFP = Small Formfactor pluggable (Module bay)

Please note: Some interfaces are optional and require specific transceivers or expansion modules to be installed on the card, as well as appropriate licensing options to unlock them.

Please contact our sales department or technical support for questions to the available license and hardware options.

3   Hardware

3.1   Definition

The **PXI 6141 GÖPEL electronic GmbH** Ethernet board is a programmable, intelligent multibus controller providing various communication interfaces for vehicle network testing and general control applications.

SFP modules can be implemented to use the board for all supplied interfaces.

SFP transceiver modules - overview:

- Ethernet 10/100/1000Mbit/s
- 100/1000Base-T1 (Marvell 88Q2112)
- 100Base-T1 (TJA1100)

Generally, **PXI 6141** controller boards provide the following features:

- Trace data acquisition on all interfaces
  with precise hardware time stamps
- Trace data generation in the **pcap-ng** format
- Cyclic and event-based transmission of Unicast, Multicast and Broadcast Messages
- Diagnostics over Ethernet (DoIP)
- Up to 4x Ethernet 10/100/1000Mbit/s
- Up to 4x 100/1000Base-T1
- 600MHz Power PC with 512Mb RAM, 256MB Flash
- High flexibility by pluggable transceiver modules
- **PXI 6141** board control via PXI or Ethernet
- The 1 Gbit Ethernet interface at the front panel
  is also useable as volume data and debug interface
- Visualization of the operating states by four LEDs
  arranged at the front panel

3.2   Technical Data

3.2.1   General

The PXI 6141 controller board is a slot-in board developed for the PXI™ bus. PCI eXtensions for Instrumentation (PXI) is a modular instrumentation platform originally introduced in 1997 by National Instruments and now promoted by the PXI Systems Alliance (PXISA).

PXI™ is based on the CompactPCI™ bus, and offers all of the benefits of the PCI architecture including performance, industry adoption and COTS technology. PXI offers a stable mechanical form factor (CompactPCI) and is standardized by an industry consortium that defines hardware, electronics, software, power supply and cooling requirements. In addition, PXI™ has integrated timing and synchronization mechanisms that enable clock and trigger signals to be distributed between the bus stations. PXI™ is a promising technology and has been developed to be able to react quickly and easily to changes in test, measurement and automation requirements.

The PXI 6141 controller board operates as PXI slave, therefore the board may be plugged into any desired slot of a PXI chassis (except slot 1). The PCI Plug & Play auto detection mechanism is supported by the PXI 6141 controller board. No jumper configuration is needed for PXI integration.

CompactPCI and PXI products are interchangeable, i.e. they can be used in either CompactPCI or PXI chassis. However, certain clock and triggering capabilities may be lost due to operation in the other rack. For example you could mount a CompactPCI network interface controller in a PXI rack to provide additional network interface functions to a test stand. Conversely, a PXI module installed in a CompactPCI chassis would not be able to use its additional clock and triggering features of the PXI module.

The PXI 6141 controller board is already prepared for use in a PXI Express hybrid slot that supports both PCI and PCI Express.

3.2.2   Dimensions

The PXI 6141 controller board is a 3U standard module and occupies one slot width.

Board dimensions without front plate and handle:

- ♦ PXI 6141: 160 mm x 100 mm (L x W)

3.3   Structure and Function

3.3.1   General

A powerful 600MHz AMCC 460EX PowerPC forms together with the I350 and FPGA the core ofthe PXI **6141** controller board. As a 32Bit RISC CPU, the Power-PC is based on the Book-E Enhanced PowerPC architecture, which, thanks to Superscalar technology, enables the simultaneous loading of two integer instructions and optimizes the processing sequence of the individual instructions in the instruction pipeline. With its highly optimized, double precision floating point unit, this processor provides the processing power required to run complex rest-of-bus simulations on multiple interfaces. The board also includes 512MB of high-speed DDR2 RAM clocked at 400MHz and 256MB of Flash memory, over 80% of which is available for application programs.

The PXI **6141** controller board has been developed as highly flexible multibus controller platform.

Figure 3-1: PXI 6141 – Schematic diagram
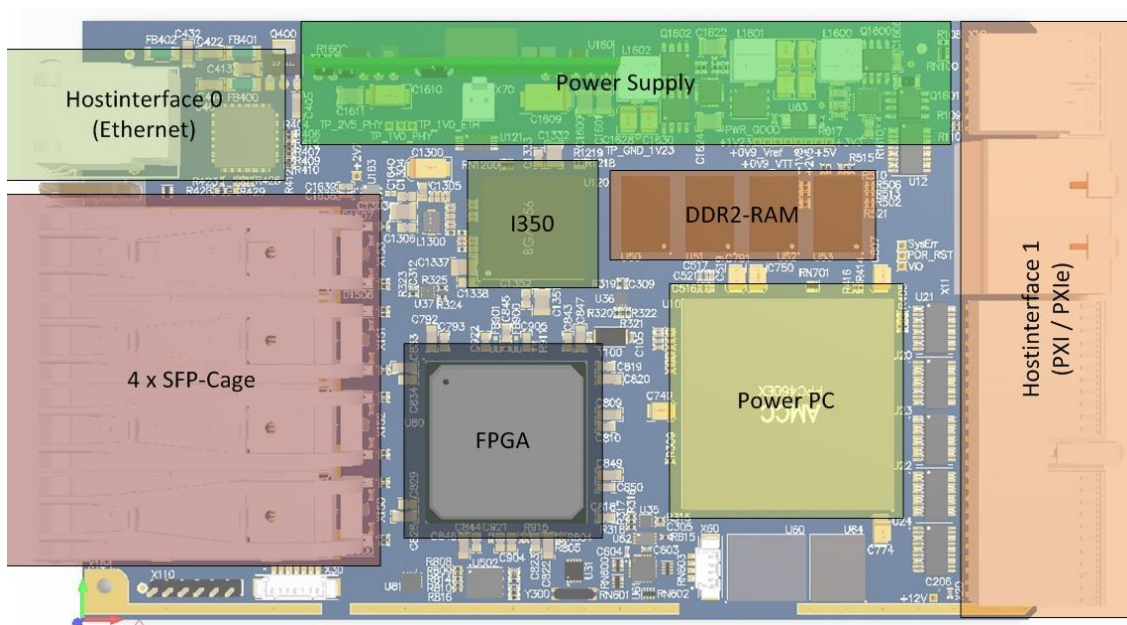
Figure 3-2: PXI 6141 – Interface overview

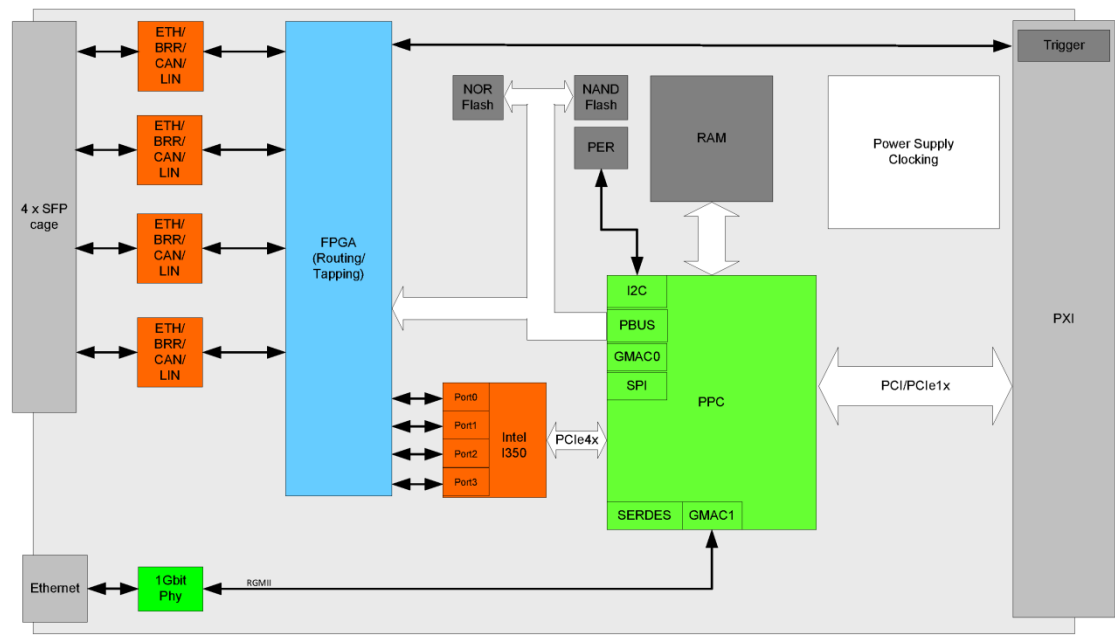| 0	SFP Slot 0
1	SFP Slot 1
2	SFP Slot 2
3	SFP Slot 3
4	Host interface 0 (Ethernet)
5	Host interface 1 (PXI)

Figure 3-3: PXI 6141 Block diagram

3.3.2 Addressing

PXI 6141 boards have a 1GBit Ethernet and a PXI interface.

Both interfaces can be used for the communication of the unit with the host PC.

In case of using the **Ethernet** interface, the board can be controlled via the **Default IP Address** 192.168.1.62, **Port 5134** which can be changed if required (see also Driver Installation/ Ethernet).

In principle, there are two ways of doing this:

- Hardware Explorer: Select the device, under **Device** set the required **IP Address**; the new **IP Address** is effective after restart
- G API Command **G_Common_Ethernet_IpAddress_Set**; the new **IP Address** is effective after restart

PXI racks have their own geographical slot addressing of the backplane. The numbering starts with **1** and is visible on the front of the housing. Slot 1 must always be equipped with an embedded controller or an MXI card.

A **PXI 6141** board can read out this geographical slot address.

3.3.3 Isolation

Electric surges can harm expensive test equipment and lead to unreliable test results. Electric isolation protects against overvoltages and can suppress dangerous current surges. It also prevents ground loops, which are responsible for data errors due to ground potential differences.

The signal lines of the SFP Modules are capacitively decoupled.

3.3.4 Status LEDs

The LEDs located on the front panel provide information about the current operating state of a **PXI 6141** board:
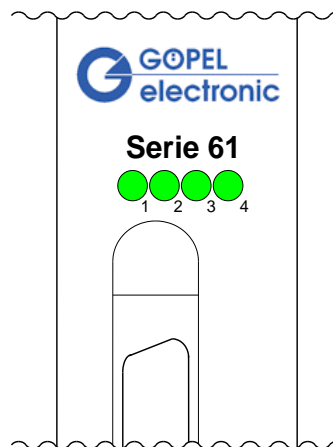
Figure 3-4:
Status LEDs

The table below describes the meaning of the LED states:

LED 1	LED 2	LED 3	LED 4	Remarks
Permanently ON				Controller does not run (Error!)
Alternately blinking				Bootloader software runs
	blinking			Firmware runs
ON (shortly)				State during execution of a Firmware command
			ON	Ethernet connection established

3.3.5 SFP LEDs

The LEDs located next to the SFP slots provide information about the Ethernet connection of each port:

Figure 3-5:
SFP LEDs

The states of the LEDs are explained in the following overview:

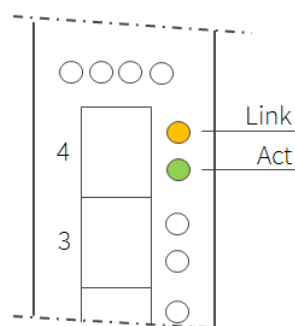|	Link LED	Act LED
Off	No Link	No data transfer
Lights orange	Link with 10/100 Mbit/s	Package is received
Lights green	Link with 1000 Mbit/s	Package is sent

3.3.6 Ethernet Host

The Ethernet Module is using a Triple-Speed Transceiver in half duplex as well as full duplex operation.
An Ethernet cable of category "CAT-6" or higher should be used for data transmission.

Properties:

- Hot pluggable module
- Temperature range: 0°C .. 85°C
- Connection via RJ45 plug
- Data rate: 10/100/1000Mbit/s
- Max. cable length up to zu 100m

Pin assignment of the RJ45 plug:
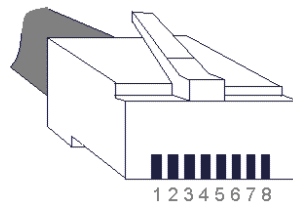
Ethernet Module:

Pin	**Signal**
Shield	Ground
1	D1+
2	D1-
3	D2+
4	D3+
5	D3-
6	D2-
7	D4+
8	D4-

3.3.7 Automotive Ethernet

Properties:

- Hot pluggable module
- Connection via RJ45 plug
- Data rate :100/1000Mbit/s full duplex
- Max. cable length up to 15m
- Unshielded Twisted Pair (UTP) cable as transmission medium
- Capacitive output coupling of the data lines

100/1000Base-T1 module:

Pin	Signal
Shield	Ground
1	TRX+
2	TRX-
3	open
4	reserved
5	reserved
6	open
7	open
8	Ground

For simple connection the D-Sub to RJ45 adapter can be used:

D-Sub adapter cable for 100/1000Base-T1 pinout:

D-Sub (plug)   RJ45

Pin	100/1000Base-T1	Pin	100/1000Base-T1
1	open	1	TRx+
2	open	2	TRx-
3	Shield	3	open
4	TRx+	4	open
5	TRx-	5	open
6	open	6	open
7	open	7	open
8	open	8	open
9	open		

 Whether the transceiver module operates in master or slave mode is determined on the TJA1100 module with the slide switch on the back:

- M = Master Mode
- S = Slave Mode

With the 88Q2112 module the master or slave mode can be set with the G-API command **G_Ethernet_Phy_Master_Slave_Mode_Set**.

3.3.8 FPGA Construction Ethernet/ Automotive- Ethernet

The following block diagram shows an overview of the handling of the TAP matrix implemented in the FPGA with the internal MII connections.

The FPGA has access to all four SFP modules, all MACs of the I350, and the internal packet generators.
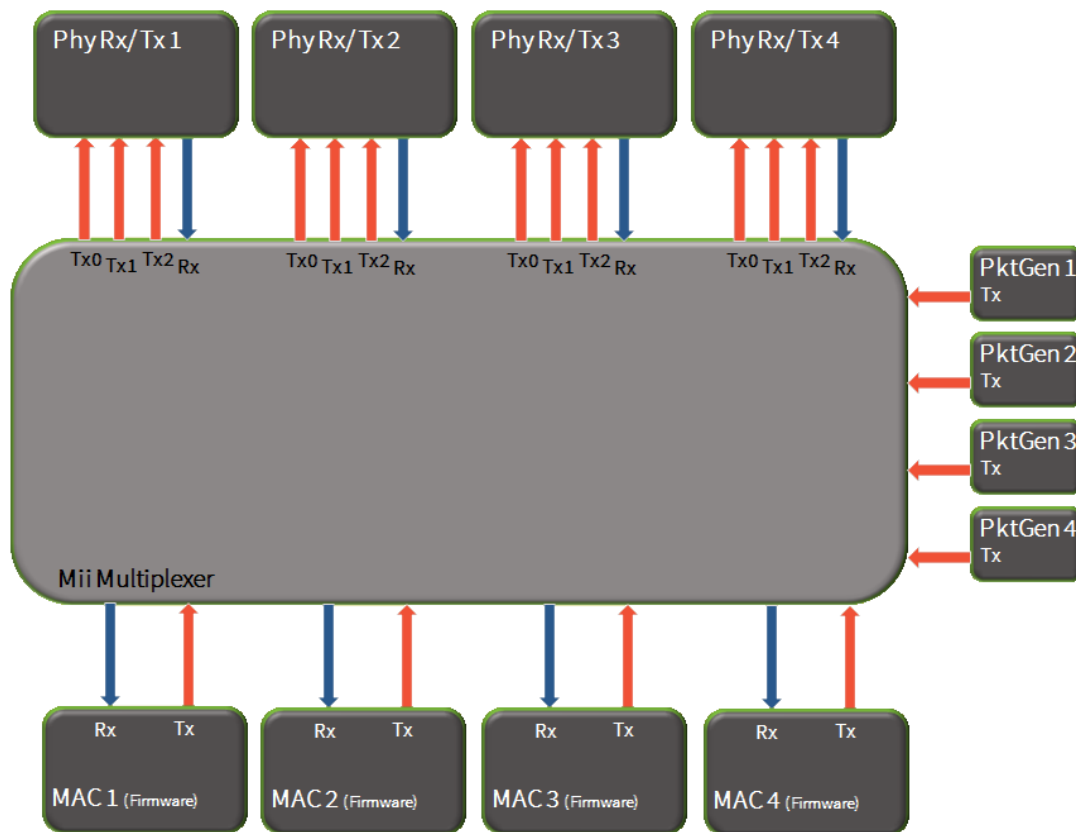

Figure 3-6: TAP-Matrix

3.3.9 Packet Generators

A **PXI 6141** board has four freely configurable Packet Generators. Each of these generators has the following features:

- Configurable packet length: 1 .. 4096 bytes
- Configurable pause between successive packets: 0ns .. $(2^{64}-1)*8$ns
- Resolution: 8ns
- Output of a configurable number of packets: 1 .. $(2^{32}-1)$ or continuous output
- Configurable data rate: 10/100/1000 Mbit/s

3.3.10 Packet filter

PXI 6141 have two packet filters, one before MAC0 and one before MAC2 (see figure 2-5).

The following conditions can be filtered:

- VLAN-TAG
- Ethernet-Type
- Next Header
- IP-source
- IP-destination
- Source-Port
- Destination-Port

Each of these filter conditions can be activated or deactivated individually. The conditions can be OR- or AND- operated combined. Each filter set can also be configured as a positive or negative filter. In each packet filter, 10 of these filter sets are integrated.

3.3.11 GMII Switch

Each SFP has a GMII switch. This switch can switch up to three inputs with the following distribution scheme:

- Round Robin
- Priority on Source 0
- Priority onSource 1
- Priority onSource 2

If the priority is on source X, this input is always preferred. If no datal are received here, the system jumps to source X+1. As soon as data come to source X again, it is prioritized again. If there are no dataat source X and X+1, the third input (X+2) is jumped to.

3.3.12 TAP Matrix

In order to design the TAP matrix for a common transmission standard, the GMII transmission standard is used internally in the FPGA. The TAP matrix allows you to connect any data source to any data sink.

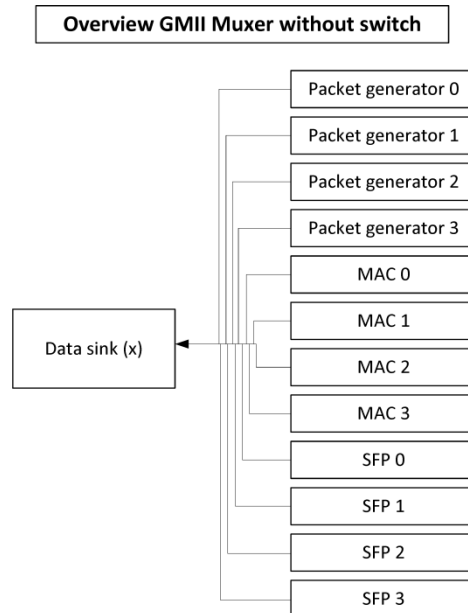Each data sink is preceded by the following multiplexer:

Figure 3-7:
Multiplexer

"Data sink (x)" in this image represents the pluggable Ethernet modules 0 .. 3, Automotive-Ethernet modules 0 .. 3 and the internal MACs 0 .. 3.

This TAP matrix makes it possible, for example, to loop an Automotive-Ethernet connection through the FPGA with SFP0 and SFP1 without influencing the communication between the two UUTs, and simultaneously record the RX data via the internal MACs 0 and 1.

4   Software

To integrate the PXI **6141** boards into your own applications the following possibilities are available:

- Programming via G-API
- UserCode Programming
- Programming with LabVIEW

4.1 Programming via G-API

The G-API (GÖPEL-API) is the C-based user interface for GÖPEL **electronic** hardware under Windows.
It provides a wide, hardware independent command set for CAN, CAN-FD, LIN/ KLine, MOST, FlexRay, Ethernet, LVDS, SENT, ADIO and Diagnostic services. No matter whether a PXI/ PCI, USB or Ethernet device is used, the commands remain the same.

The hardware abstraction introduced with the G-**API** gives the test application parallel access to the hardware, allowing one application to access multiple hardware interfaces. On the other hand, several applications can also access the same hardware interface in parallel.

Another feature introduced by the G-**API** is the asynchronous hardware access. This means no execution blocking for pending firmware commands. The command acknowledgement is provided via a callback mechanism.

With the **Hardware Explorer** (see also Ethernet), **GÖPEL electronic** provides an efficient hardware configuration and management tool, offering users an easy way to manage their hardware configurations and identifying specific hardware interfaces by logical names. Using logical interface names in the application saves from rebuilding the application when porting it to another interface or controller board, as the interface can be easily reassigned in the Hardware Explorer.
Furthermore, the **Hardware Explorer** provides a simple means of testing the interaction between hardware and software by executing the integrated self-tests.

> Please consult the G-**API** documentation for further information. This documentation and the installation software are located in the *G-API* folder of the supplied "Product Information" CD.

4.2 UserCode Programming

PXI 6141 controller boards can execute user programs direct on their PowerPC processor. This requires the UserCode run-time module being enabled.

The UserCode run-time module is an option for PXI 6141 boards (plus other GÖPEL devices) and requires one license per unit.

Executing programs directly on the PowerPC improves the real-time performance remarkable and frees up PCI bandwidth on the host system.

Therefore GÖPEL electronic has ported and enhanced by additional on-board functionality their C-programming user interface called G-API from Windows® to the QNX Neutrino real-time operating system.
The QNX Neutrino real-time operating system is based on micro kernel architecture, providing clear separation between the kernel and each individual application.
This allows user applications to run in a separate virtual memory space, which ensures safe test execution and improves reliability.

The UserCode run-time module uses a superset of the G-API commands for Windows® ensuring an easy migration of existing program source code. Additional functions will provide access to event notifications, timer tasks, the FLASH file system and other RT OS resources as well as standard C libraries

The PowerPC processor uses big-endian byte order which must be taken care of when writing or porting code for the UserCode Run-time module. For smooth migration from little to big-endian, a library of conversion macros is provided with the Net2Run IDE development system.

With the Net2Run IDE development system, GÖPEL electronic provides a complete tool chain for creating UserCode programs and for their direct execution on PXI 6141 boards.

The Net2Run IDE development system is based on Eclipse IDE and contains the QNX Neutrino Command Line Tools (CLT), including PowerPC-Compiler, Linker and Debugger.

UserCode programs can be downloaded and debugged direct from
Net2Run IDE via an Ethernet connection.

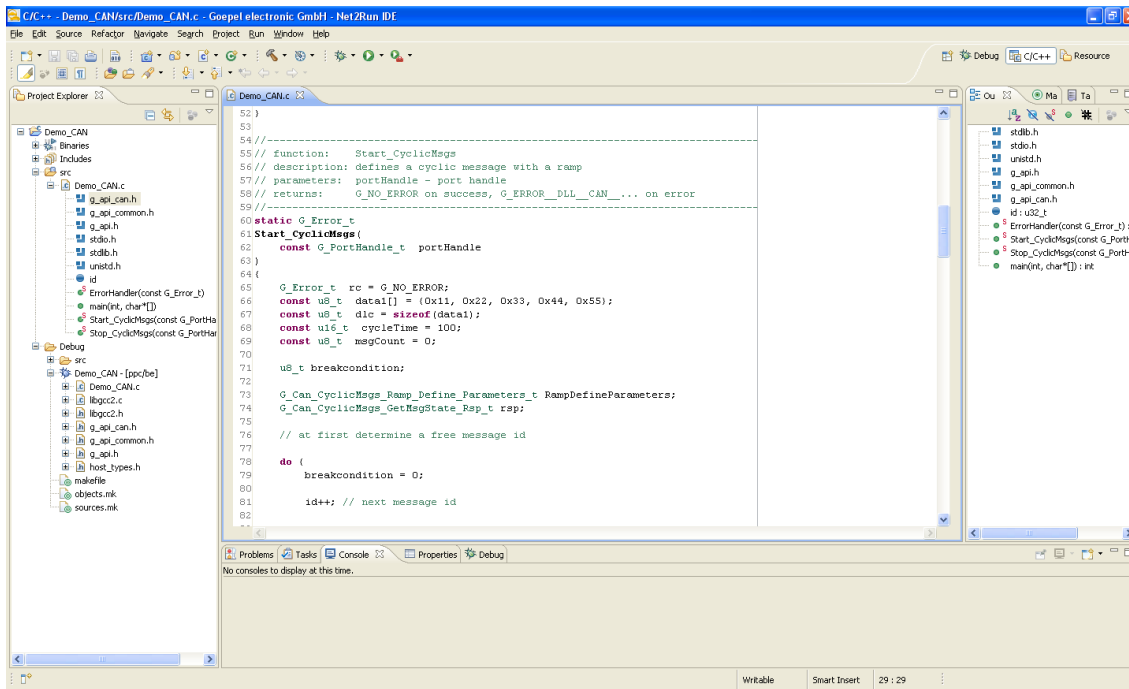The figure below shows the **Net2RunIDE** development system:

Figure 4-1: Net2Run IDE Window

Please consult the **G-API** documentation for further information.
This documentation and the installation software are located in the
G-API folder of the supplied "Product Information" CD.

4.3   Programming with LabVIEW

4.3.1   LabVIEW via the G-API

The supplied CD contains VIs for activating PXI **6141** boards under LabVIEW.

These LabVIEW VIs use the functions of the GÖPEL **G-API**.

4.4 Additional Software Interfaces

4.4.1 FS

The Software Interface "FS1" (File System) allows, amongst others, creating, copying, deleting, executing and searching of files on the hardware.
Thus, it allows uniform access to the OnBoard File System.

4.4.2 Net2Run

The Software Interface "Net2Run" (Net2Run1 .. Net2Run4) serves for the creation, configuration and execution of Residual bus simulations. Several bus interfaces for CAN, LIN and FlexRay networks can be simulated simultaneously and continuously.
The "Net2Run" interface supports loading and executing of so-called Residual bus simulation files (*.rbs). These are preconfigured command sequences containing a static Residual bus simulation.
The corresponding files are created by means of the "Net2Run" Configurator Tool.

"Net2Run" is subdivided into several Software modules, strongly leaning to "AUTOSAR".

The following Software modules do exist:

- COM
- PDU-Router
- CAN-Interface
- LIN-Interface
- FlexRay-Interface
- PDU-Multiplexer
- CAN-NM
- FlexRay-NM

Hence, the routing of PDUs of e.g. CAN1 to CAN2, CAN1 to LIN3 or FlexRay2 to CAN4 is possible (PDU-Gateway). The routing of individual signals can be realized by a COM-Signal-Gateway. In order that several independent Residual bus simulations can be executed on one card (e.g. one Residual bus simulation on CAN1, CAN2, CAN3 and CAN4 each), several "Net2Run" Interfaces do exist (4).

4.4.3 Sequence

The Software Interface "Sequence1" allows recording and playing of Firmware commands as a command sequence, short "Sequence". A sequence can also be saved permanently under any name on the card. By using its name, this Sequence can be loaded again and played. The automatic loading of a Sequence after switching on the board e.g. allows the automatic configuration and starting of a Residual bus simulation (in the case the required commands are included in the Sequence).

4.4.4 UserCode

The Software Interface "UserCode1" allows the OnBoard execution of user programs (see also **UserCode Programming**)**.**

For the communication between OnBoard programs and the Host, Message-FIFOs do exist.

Each side (OnBoard program or Host) can create, write to or read from a Message-FIFO.

Each FIFO can be read and written from both sides. For consistency it is recommended to have a separate FIFO for each direction. So that one side only writes to and the other side only reads from a FIFO.

5 Disposal

5.1 Disposal of used Electrical / Electronic Equipment

The device implements the following EU directives:

- 2012/19/EU (WEEE) Waste Electrical and Electronic Equipment and
- 2011/65/EU on the restriction of the use of certain hazardous substances in electronic equipment (RoHS directive)

At the end of the life of the device, this product must not be disposed of with other household waste. The improper disposal of this type of waste can have a negative impact on the environment and health due to the potential hazardous substances in electrical and electronic equipment. Dispose of the product at a suitable collection point.

When disposing of the device in countries outside the EU, local laws and regulations must be observed.

5.2 Disposal of used Disposable Batteries / Rechargeable Batteries

At the end of the service life of disposable batteries / rechargeable batteries, these must not be disposed of with the normal household waste. Dispose of the disposable batteries / rechargeable batteries at a recycling center for disposable batteries and rechargeable batteries.

Please dispose of only discharged disposable batteries / rechargeable batteries.