Product Specification

PXI / PCI 3072

LIN/ K-Line Interfaces

User Manual

Version 1.8

GOPEL electronic

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1 Installation of the Board

1.1 Hardware Installation

Before beginning with the hardware installation you have to ensure that your system is switched off and disconnected from the mains supply.

Please refer also to the user manual of your PXI/ PCI system for additional installation instructions that possibly have to be followed.

Electro Static Discharge (ESD) can harm your system and destroy electronic components. This can lead to irreparable damage on both the PXI/ PCI 3072 board and the system hosting the board as well as to unexpected malfunction of your test system.
Therefore do not touch the board surface or any connector pins and electronic components.

The PCI™-, CompactPCI™- or PXI™ system is to be opened according to its conditions. A free slot is to be selected in your system.
Now, the slot cover is to be taken away from the slot selected. To do this, unscrew the fixation screws and remove the cover from the slot.

(If it is necessary to exchange transceiver modules, pay attention to the general rules to avoid electrostatic charging, see the warning above. Transceiver modules must never be removed or mounted with the power switched on!
Additionally, the right alignment is absolutely required.)

Insert the board carefully into the prepared slot. For the PXI board, use the lever at the front plate in order to push in the board finally.

When the board has been inserted properly, it is to be fixed by means of the screw(s) at the front plate.
Now, the board has been installed correctly.

Afterwards, carry out the operations required at the system to make it ready for operation anew.

1.2 Driver Installation

1.2.1 Windows Device Driver

PXI/ PCI 3072 boards can be operated under Windows® XP as well as under Windows®7/ 64 bit.

Due to the plug and play capability of Windows®, for every newly recognized hardware component a driver installation is started automatically via the hardware assistant.
The hardware assistant can carry out the installation of the device driver by using the *inf* file contained in the *GPxi3072* folder on the supplied CD.

If necessary, you can find the required *inf* files as follows:

- *GPxi3072.inf* for Windows® 2000/ XP
  in the *Win2000 (Version xx)* folder
- *GPxi3072_x64.inf* für Windows®7/ 64 bit
  iin the *Win7_x64 (Version xx)* folder

It is not absolutely essential to restart the system.

If you want to create your own software for the boards, you possibly need additional files for user specific programming (**.LLB*, **.H*).
These files are not automatically copied to the computer and have to be transferred individually from the supplied CD to your development directory.

This step is only required in case you do not use the G-API (see also Control Software).

1.2.2 VISA Device Driver

First step

Copy the *VISA (Version xx)* directory from the *GPxi3072* folder of the delivered CD to your hard disk.
(Recommendation: Complete directory to *C:* \)

Second step

Windows2000, WindowsXP :

Due to the plug and play capability, for every newly recognized hardware component a driver installation is started automatically via the hardware assistant. Follow the instructions. Enter as target directory the one which contains the *PXI3072_NT5.inf* file (according to recommendation: *C:* *VISA (Versionxx* *Installation*).

LabViewRT :

For operating PXI/ PCI 3072 boards under the RT operating system, use the *P3072_RT.inf* file from the *C:* *VISA (Version xx)* *Installation* directory.

Copy this file to the *ni-rt* *system* folder of the embedded controller (recommendation: copy by the NI Measurement Explorer).

If you intend to create a *startup.rtexe* later, copy also the *cvi_lvrt.dll* file to the *ni-rt* *system* folder.

Third step:

Reboot your computer to complete installation.

After driver installation, you can check whether the boards are properly imbedded by the system:

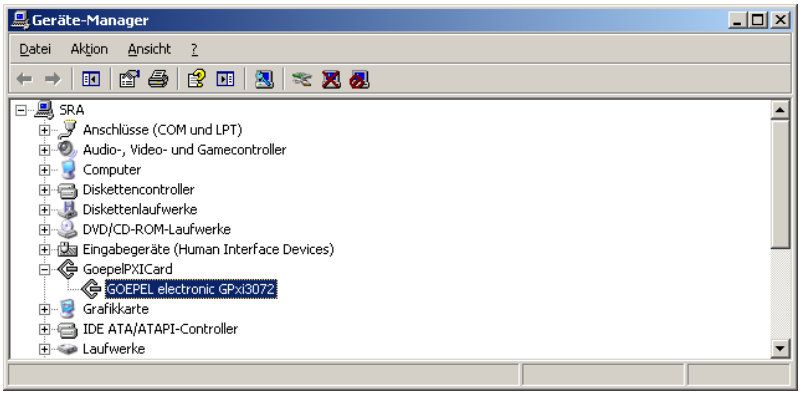

Figure 1-1: Windows

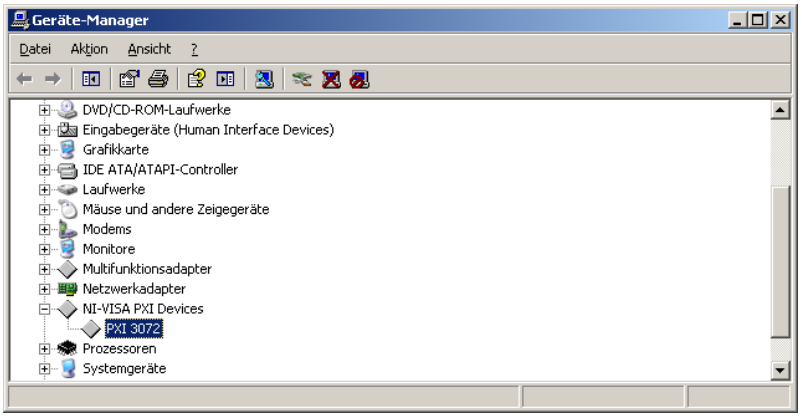

Figure 1-2: VISA

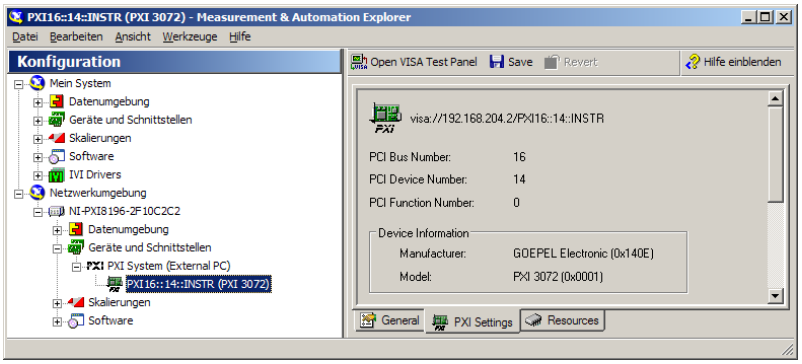

Figure 1-3: VISA RT

2 Hardware PXI / PCI 3072

2.1 Definition

The PXI 3072/ PCI 3072 multi-interface-boards are communication boards of GOEPEL electronic GmbH.

These boards with up to three LIN or K-Line interfaces are used in general control technology, especially for applications in automotive technology.

In this User Manual, Controller ALWAYS means the microcontroller assigned to a LIN or K-Line interface
(with the exception of the “LIN Controller” designation on the front panel for the entire board).

Figure 2-1: PXI 3072

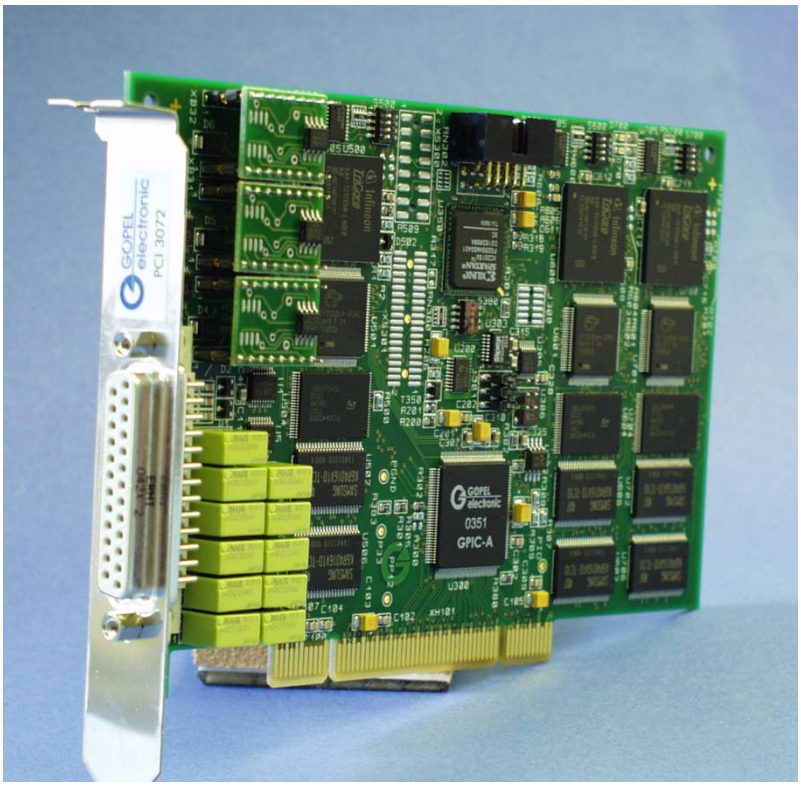

Figure 2-2: PCI 3072

2.2 Technical Data

2.2.1 General

The PXI 3072 communication board is a plug-in board developed for the PXI™ bus (**P**CI e**X**tensions for **I**nstrumentation). Basis of this bus is the CompactPCI™ bus.

The board can be plugged into any desired slot of a CompactPCI™ or PXI™ system (except for slot 1). It can be definitely identified also in the case that several boards of this type are used in the same rack.

The PCI 3072 communication board is a PC plug-in board for the PCI Local Bus Rev. 2.2.
It can be operated at any PCI slot (32 bits, 33 MHz, 3.3 V)

Both boards do not have jumpers for hardware detection and are automatically integrated into the respective system.

2.2.2 Dimensions

The dimensions of both boards correspond to standard dimensions of the accompanying bus system:

- PXI 3072 Multi Interface Board: 160 mm x 100 mm (L x W)
- PCI 3072 Multi Interface Board: 168 mm x 106 mm (L x W)

2.2.3 PXI 3072/ PCI 3072 Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remarks
V_{CC}	LIN system voltage		12		V	
	External trigger output		5		V	I_{load} - max. 25mA
	External trigger input	3.3		50	V	
	LIN transmission rate		19.2	22	kBaud	
	K-Line transmission rate		10.4	115	kBaud	

2.3 Construction

2.3.1 General

An ASIC is used as the interface to the PCI or cPCI bus on the PXI/ PCI 3072 boards. It includes all the function blocks required for the communication with the computer bus.

The PCI 3072 communication board does not have a PXI interface. To exchange trigger signals with other GOEPEL electronic PCI boards despite of that, an additional plug connector is on this board with two lines configurable as input or output (XS2 in Figure 2-7).

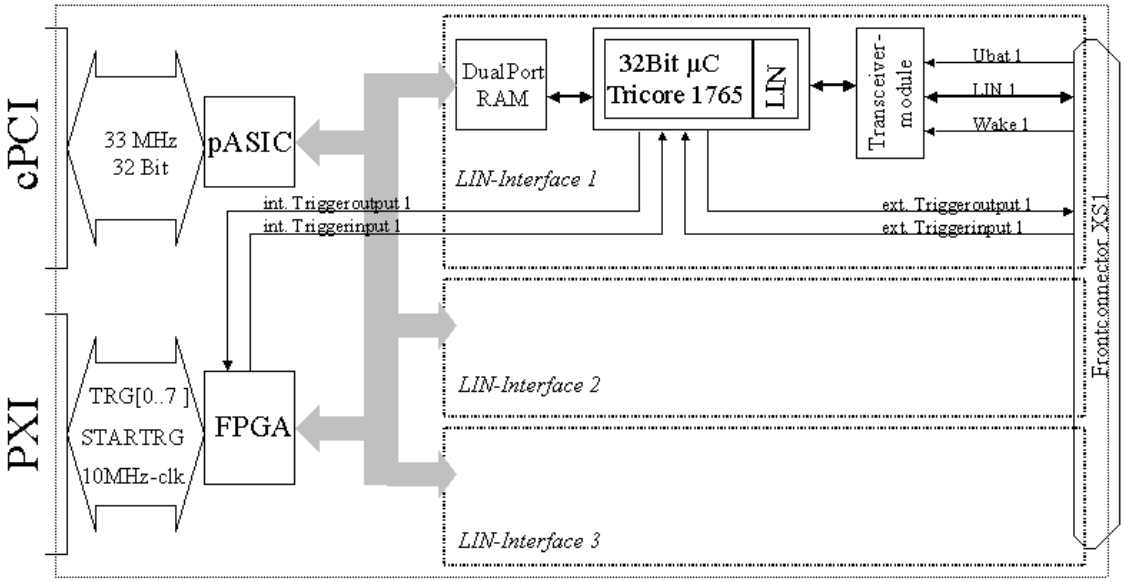

Figure 2-3: Block diagram of a PXI 3072 Communication board

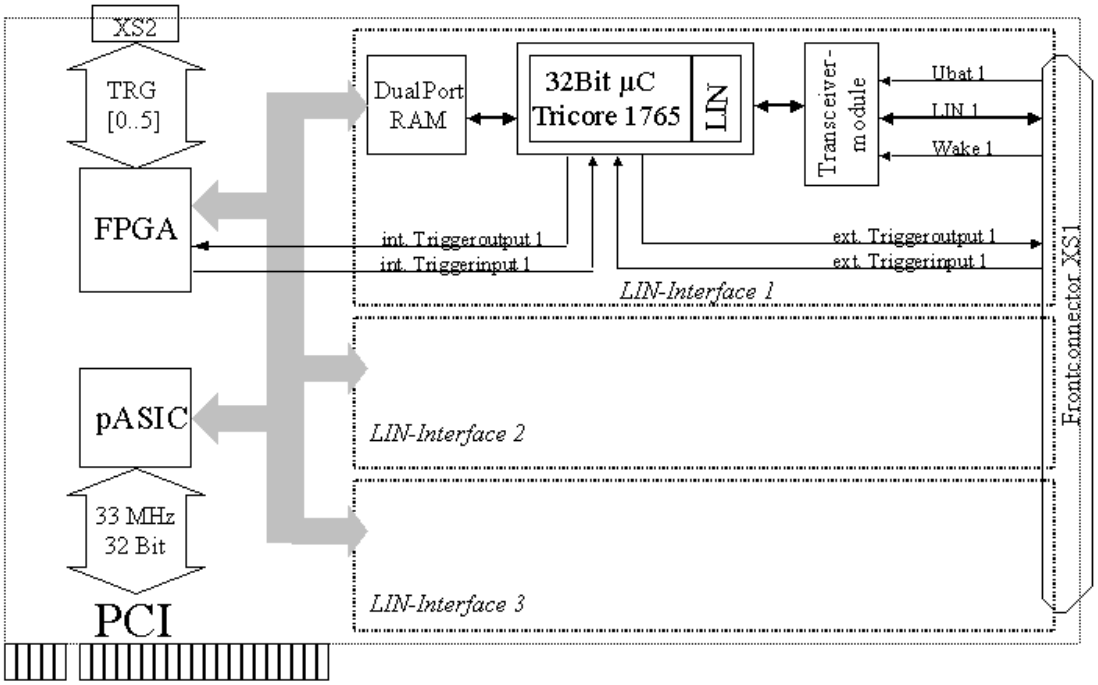

Figure 2-4: Block diagram of a PCI 3072 Communication board

2.3.2 Addressing

PXI 3072: PXI racks do have an own geographical slot addressing of the backplane. Numbering starts with 1 and can be seen at the cover's front side. Mount always an embedded controller or an MXI card at slot 1.

The PXI 3072 board can read out this geographical slot address. For that the belonging FPGA file has to be loaded to the XILINX (see the XilinxDownload functions for different drivers in the Control Software section).

PCI 3072: PCI racks do not have an own geographical slot addressing. There is a separate DIP switch (DIP 4 in Figure 2-7) for clear identification of the board in a system with several PCI 3072 boards. You can select up to 16 addressing variants by this.
The corresponding binary value (0..15) set with the DIP 4 switch can be read out by the delivered software.

2.3.3 Communication Interfaces

Up to 3 x LIN-Interface Version 2.0 or
Up to 3 x K-Line Interface (ISO 9141)

The following figure shows the output circuitry of a PXI/ PCI 3072 board between the transceiver modules and the frontal plug connector:

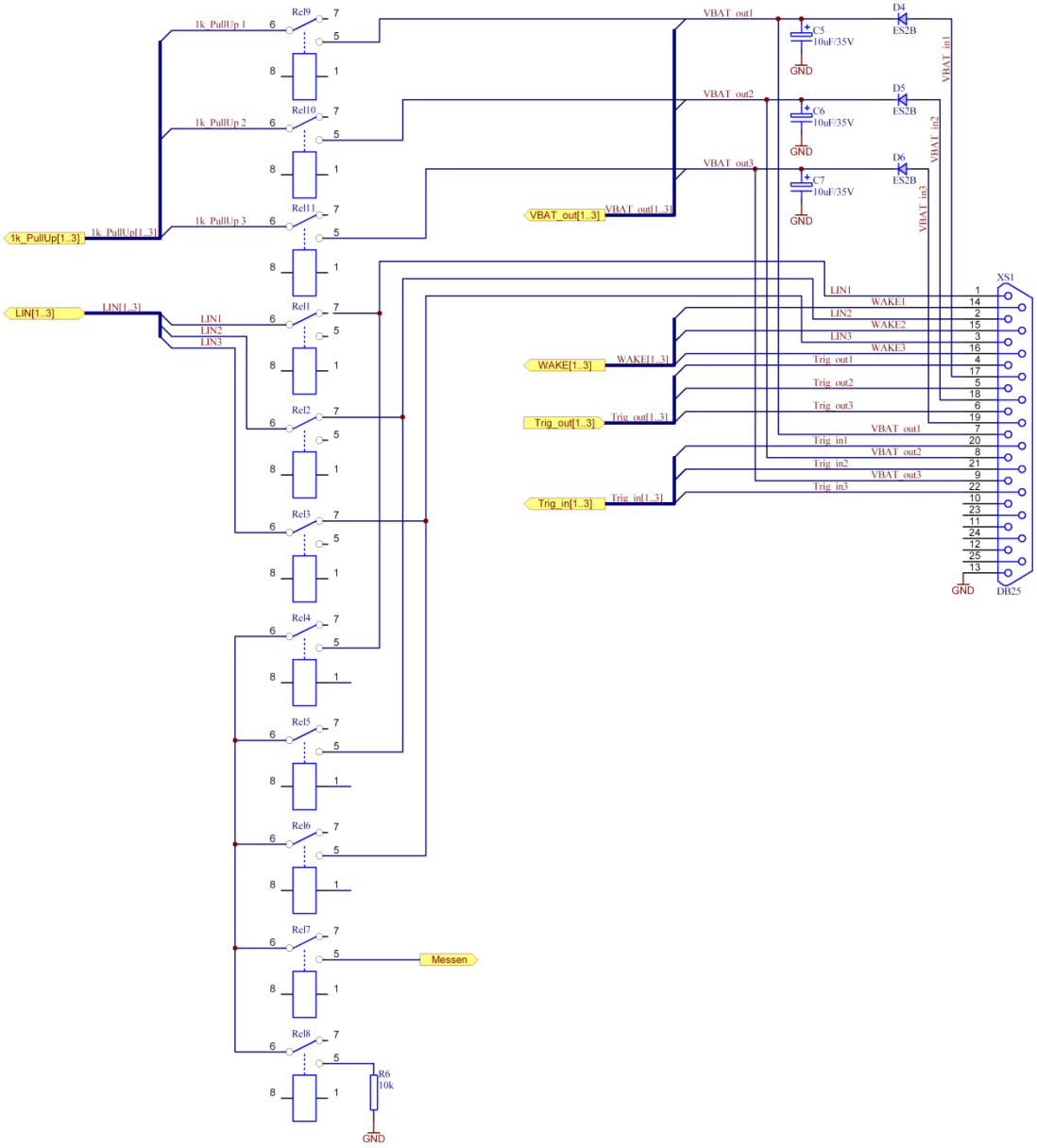

Figure 2-5: Detail of PXI 3072, PCI 3072 Output Circuit Diagram

If it is necessary to change transceiver modules, take care that the square pins (Pin1) of the socket and the transceiver module lie about each other.

The orientation of the transceiver modules is different in the case of PXI 3072 or PCI 3072 boards (see Figure 2-6 and Figure 2-7)!!!

LIN:

The transceivers are designed as plug-in modules. Generally, the TJA1020 of Philips is used for this type of transceicer.

For the standard design of the transceiver modules, it is possible to change over between Master and Slave configuration per software using the relays Rel9 for LIN1, Rel10 for LIN2 or Rel11 for LIN3.

The pull-up resistors for LIN are located on the transceiver modules.

Via the V_{Bat} contacts the power supply of the transceiver modules is connected. According to the LIN specification, this power supply is to be carried out via a reverse-connect protection diode and a support capacitor (so the V_{Bat} voltage is fed by VBAT_in 1..VBAT_in 3).
The voltage fed at the power supply (voltage) pin should not exceed the transceiver's scope (for TJA1020, the upper V_{BAT} voltage limit is 27 V).

The VBAT_out 1..VBAT_out 3 connections are monitoring outputs to measure the real voltage at the transceiver, possibly to compare this voltage with the LIN signal level.

For special control and measuring tasks, both communication boards are provided with a hardware trigger output and input. Please refer to the GOEPEL Firmware documentation regarding their function.

In addition, PXI/ PCI 3072 boards offer the possibility to separate the LIN communication bus from the corresponding test object (device or unit under test) via the relays 1..3.

The relays 4..6 allow the interconnection of the three LIN interfaces to a common bus on the board (see Figure 2-5).

K-Line:

The transceivers are designed as plug-in modules. Generally, the L9637 of ST is used for this type of transceicer.

Via the V_{Bat} contacts, the power supply of the transceiver modules is connected. The voltage fed at the power supply (voltage) pin should not exceed the transceiver's scope (for L9637, the upper V_{BAT} voltage limit is 36 V).

To bridge the reverse-connect protection diode for V_{Bat} for LIN, the V_{BAT} voltage can be fed via VBAT_out 1..VBAT_out 3.

2.3.4 Assembly

Figure 2-6 and Figure 2-7 show schematically the component side of the boards. You can see the positions of the transceiver modules, plug connectors and DIP switches.

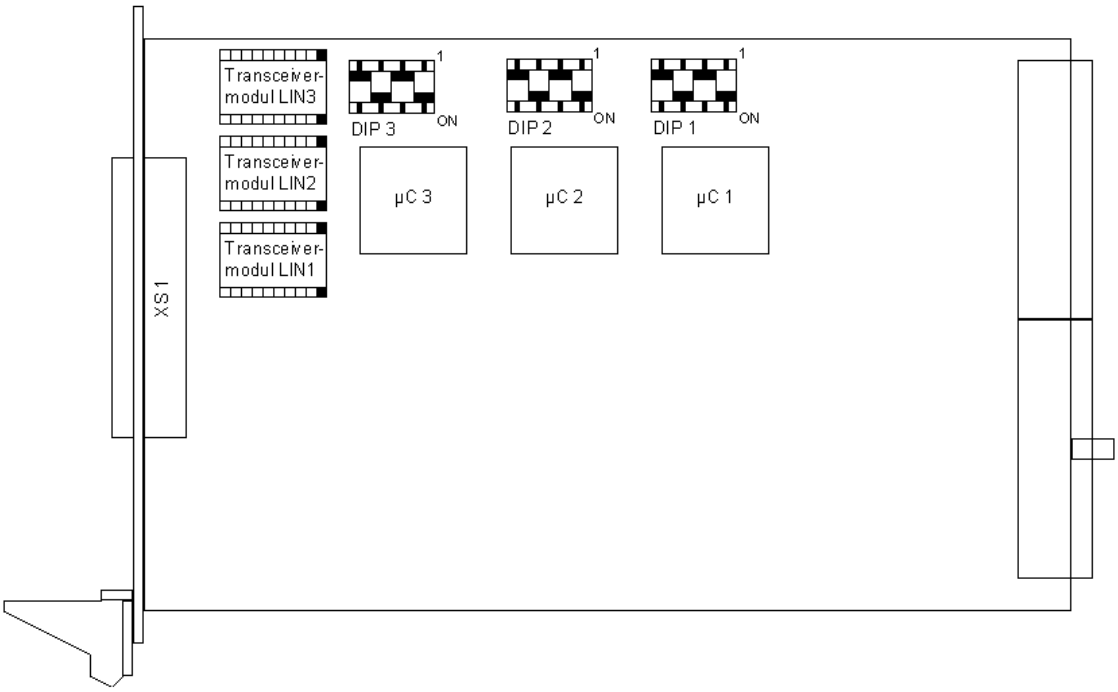

Figure 2-6: Component side of a PXI 3072 Communication board (schematically)

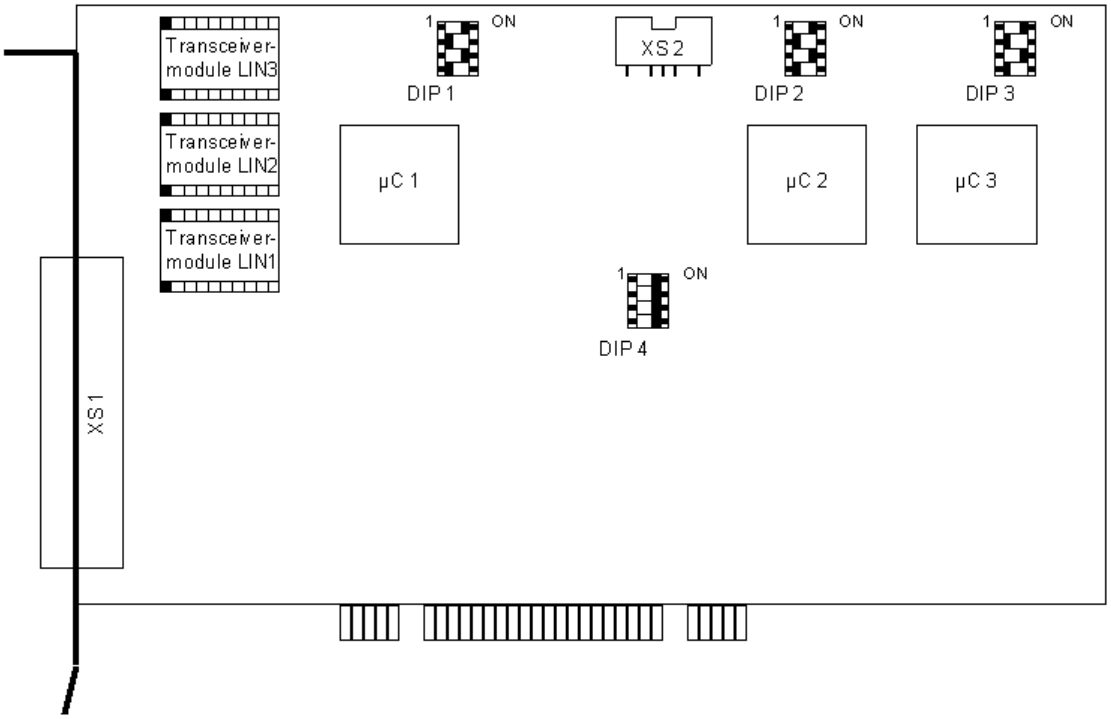

Figure 2-7: Component side of a PCI 3072 Communication board (schematically)

The configuration elements of Figure 2-6 and Figure 2-7 are explained in the following table:

LIN1	Transceiver module for LIN1/ KLine1
LIN2	Transceiver module for LIN2/ KLine2
LIN3	Transceiver module for LIN3/ K-Line3
DIP1..3	DIP switches of the PXI/ PXI 3072 boards to configurate the micro controllers. **Do NOT change the settings!**
DIP 4	This DIP switch on a PCI 3072 board is for clear identification of the board (analogously to "geographical addressing" of the PXI specification) in a system with several PCI 3072 boards. You can select up to 16 addressing variants this way (0..15). The corresponding binary value set with the DIP 4 switch can be read out by the delivered software.
XS2	Plug connector to exchange trigger signals with other GOEPEL electronic PCI boards

2.3.5 Assignment Frontal Plug Connector

Type: DSub 25 poles socket

The interfaces are provided via this plug connector at the frontal edge of the PXI/ PCI 3072 communication boards.

The assignment of both boards is identical according to the following table:

XS1 pin	Signals name	Remarks
1	LIN1/ K-Line1	
2	LIN2/ K-Line2	
3	LIN3/ K-Line3	
4	Trigger output LIN1	TTL signal
5	Trigger output LIN2	TTL signal
6	Trigger output LIN3	TTL signal
7	VBAT 1 Out	
8	VBAT 2 Out	
9	VBAT 3 Out	
10	-	not assigned
11	-	not assigned
12	-	not assigned
13	Gnd	Ground potential
14	Wake1	
15	Wake2	
16	Wake3	
17	VBAT 1 In	
18	VBAT 2 In	
19	VBAT 3 In	
20	Trigger input LIN 1	Signal level: 5V..VBAT
21	Trigger input LIN 2	Signal level: 5V..VBAT
22	Trigger input LIN 3	Signal level: 5V..VBAT
23	-	not assigned
24	-	not assigned
25	-	not assigned

For LIN, the PINs 14/ 15/ 16 may be connected with the WAKE lines (depending on the transceiver).

2.4 Delivery Notes

PXI/ PCI 3072 boards are delivered in the following basic variant:

- 3x LIN interface,
  to be configured as master or slave by software.

Each interface of this basic variant can also be designed as KLine-interface.

In addition to selecting an interface, the type of the corresponding LIN/ K-Line transceiver as well as the required Functionalities for each LIN/ K-Line interface must be selected.

3 Control Software

There are three ways to integrate PXI 3072/ PCI 3072 hardware in your own applications:

- Programming via G-API
- Programming via DLL Functions
- Programming with LabVIEW

3.1 Programming via G-API

The G_API (GOEPEL-API) is the favored user interface for this GOEPEL hardware.

You can find all necessary information in the *G-API* folder of the delivered CD.

3.2 Programming via DLL Functions

Programming via DLL Functions is possible also in future for existing projects which can not be processed with the GOEPEL electronic programming interface G-API.

We would be pleased to send the GOEPEL Firmware documentation to you on your request. Please get in touch with our sales department in case you need that.

The GPxi3072 and PXI3072 expressions used in the following function description stand for PXI 3072/ PCI 3072.

For the used structures, data types and error codes refer to the headers – you find the corresponding files on the supplied CD.

In this User Manual, Controller ALWAYS means the microcontroller assigned to a LIN or K-Line interface
(with the exception of the “LIN Controller” designation on the front panel for the entire board).

3.2.1 Windows Device Driver

The DLL functions for programming using the Windows device driver are described in the following chapters:

- DriverInfo
- DLL Version
- XILINX Download
- XILINX Write Data
- DPRAM Write Instruction
- DPRAM Read Response
- DPRAM Read Monitor
- Reset Port

3.2.1.1 DriverInfo

The GPxi3072_GetDriverInfo function is for the status query of the hardware driver.

Format:

```
int GPxi3072_GetDriverInfo(GPxi3072_StructDriverInfo *pDriverInfo);
```

Parameters:

Pointer, for example pDriverInfo, to a data structure
For the structure, see the *GPxi3072.h* file on the supplied CD

Description:

The GPxi3072_GetDriverInfo function returns information regarding the status of the hardware driver.

For this reason, the address of a pDriverInfo pointer has to be transferred to the function.
The structure pDriverInfo is pointing to is filled with various information within the function.

3.2.1.2 DLL Version

The GPxi3072_DLL_Version function is for the version number query of the DLL.

Format:

```
int GPxi3072_DLL_Version(unsigned long *pVersion);
```

Parameter

Pointer, for example pVersion, to the Version number

Description:

The GPxi3072_DLL_Version function returns the version number of the *GPxi3072w.dll* as an integer value.

Example:

Version number **1.23** is returned as **123**,
and version number **1.60** as **160**.

3.2.1.3 XILINX Download

The GPxi3072_XilinxDownload function is to load an FPGA file to the XILINX.

Format:

```
int GPxi3072_XilinxDownload(unsigned long card, char *pFileName);
```

Parameters:

card

Index of the PXI/ PCI 3072 board, beginning left with 1

Pointer, for example pFileName, to the path of the FPGA file to be loaded

Description:

The GPxi3072_XilinxDownload function allows to load an FPGA file (**.cfd* extension) to the XILINX. This file serves, among other possibilities, to read the geographical slot address in the PXI Rack.

The loaded data is volatile. Therefore the function has to be executed again after switching off power.

After XilinxDownload, a delay of about 500 ms is required (as the controllers execute a power-on reset).

Then, carry out the 0x10 Software Reset firmware command for all controllers to come into the normal operating mode from bootloader mode.

3.2.1.4 XILINX Write Data

The GPxi3072_XilinxWriteData function allows the configuration and execution of functions provided by the XILINX.

Format:

```
int GPxi3072_XilinxWriteData(unsigned char *data, unsigned long *length);
```

Parameters:

Pointer, for example data , to the Write data area
(currently max. 128 bytes per command)

length

Size of the memory area data is pointing to (in bytes)

Description:

Before using the functionality of the XILINX, the corresponding FPGA file must have been loaded by GPxi3072_XilinxDownload (see XILINX Download).

The data format consists of four bytes including the command. If necessary parameter bytes can follow.

Data format:
- 1st byte: 0x48 (StartByte)
- 2nd byte: card (index of the PXI/ PCI 3072 board, beginning left with 1)
- 3rd byte: 0x00 (Reserved Byte)
- 4th byte: XILINX command

Currently supported XILINX command:

0x10 PowerOnReset for the complete board

3.2.1.5 DPRAM Write Instruction

The GPxi3072_DpramWriteInstruction is for sending a command to the selected controller.

Format:

```
int GPxi3072_DpramWriteInstruction(unsigned char *data, unsigned long length);
```

Parameters:

Pointer, for example data, to the Write data area,
consisting of Command Header and Command Bytes
(currently max. 1024 bytes per command)

length

Size of the memory area data is pointing to (in bytes)

Description:

The GPxi3072_DpramWriteInstruction function sends a command to the selected controller.

In the header of the structure data is pointing to, there is the information regarding the PXI/ PCI 3072 board and the belonging controller to be activated by this function.
Therefore these parameters are not to be given separately.

3.2.1.6 DPRAM Read Response

The GPxi3072_DpramReadResponse function is for reading a response from the selected controller.

Format:

```
int GPxi3072_DpramReadResponse(unsigned long card, unsigned long port,
                               unsigned char *data, unsigned long *length):
```

Parameters:

card

Index of the PXI/ PCI 3072 board, beginning left with 1

port

Number of the controller (1..3)

Pointer, for example data, to the Read data area, consisting of Response Header and Response Bytes (currently max. 1024 bytes per response)

length

Value of the parameter before function call:
Size of the buffer pointed by data in bytes

Value of the parameter after function call:
Number of bytes actually read

Description:

The GPxi3072_DpramReadResponse function reads back the oldest response written by the controller (1..3) into the Response area of the DPRAM.

If several responses have been provided by the corresponding controller, but not read, they are not lost but stored in the form of a list.

On calling up, the GPxi3072_DpramReadResponse function continues to supply data until this list contains no more entries.

3.2.1.7 DPRAM Read Monitor

The GPxi3072_DpramReadMonitor is for reading the monitor data of the selected controller.

Format:

```
int GPxi3072_DpramReadMonitor(unsigned long card, unsigned long port,
                              unsigned char *data, unsigned long *length);
```

Parameters:

card

Index of the PXI/ PCI 3072 board, beginning left with 1

port

Number of the controller (1..3)

Pointer, for example data, to the Read data area (max. 20kByte)

length

Value of the parameter before function call:
Size of the buffer pointed by data in bytes

Value of the parameter after function call:
Number of monitor entries actually read

Description:

The GPxi3072_DpramReadMonitor function reads the data found in the monitor area of the DPRAM.

This concerns exclusively the data provided by the controller in the Buffer reception monitor Mode.
That means, the normal DPRAM Response area is separated from DPRAM's monitor data area (Buffer reception).

20 bytes are required per monitor entry.The length given back is already divided by these 20 bytes and corresponds in this way to the number of monitor entries actually read.

3.2.1.8 Reset Port

The GPxi3072_ResetPort function is for releasing a software reset for the selected controller.

Format

```
int GPxi3072_ResetPort(unsigned long card, unsigned long port);
```

Parameters:

card

Index of the PXI/ PCI 3072 board, beginning left with 1

port

Number of the controller (1..3)

Description:

The GPxi3072_ResetPort function releases a software reset for the selected controller of a PXI/ PCI 3072 board.

This releasing procedure is executed via a separate interrupt channel, NOT via the command interpreter of the software (0x10 Software Reset firmware command).

3.2.2 VISA Device Driver

The DLL functions for programming using the VISA device driver are described in the following sections:

- Init
- Done
- Driver Info
- XILINX Download
- XILINX Write Data
- Write Data
- Read Data
- Reset Port

3.2.2.1 Init

The PXI3072_Init function is for opening VISA sessions for the system's PXI/ PCI 3072 boards including initialization.

Format:

```
ViStatus PXI3072_Init(ViUInt32 *CardCount);
```

Parameter:

CardCount

Number of the system's PXI/ PCI 3072 boards recognized by the VISA driver.

Description:

The PXI3072_Init function searches for all PXI/ PCI 3072 boards of the system and opens the required sessions.
Additionally, board internal initializations are carried out.

Therefore this function must be executed as the first step.

3.2.2.2 Done

The PXI3072_Done function closes all VISA sessions of the system's PXI/ PCI 3072 boards.

Format:

```
ViStatus PXI3072_Done(void)
```

Parameters:

none

Description:

The PXI3072_Done function closes all VISA sessions of the system's PXI/ PCI 3072 boards.

No further access to the boards is possible, then.

3.2.2.3 Driver Info

The PXI3072_DriverInfo function provides general information regarding driver and board.

Format:

```
ViStatus PXI3072_DriverInfo(PXI3072_StructDriverInfo *DriverData,
                                          ViChar *DeviceName);
```

Parameters:

Pointer, for example DriverData, to a data structure
For the structure see the *PXI3072_API.h* file of the supplied CD

DeviceName
`Array[K_DEV_MAX][K_RES_NAME_LENGTH]`
(see *PXI3072_API.h*)

Description:

The PXI3072_DriverInfo function provides information regarding the driver and the system's PXI/ PCI 3072 boards.

The DeviceName indicates the resource names registered by VISA. This information correlates with the display of NI MAX.

3.2.2.4 XILINX Download

The PXI3072_XilinxDownload function is to load an FPGA file to the XILINX.

Format:

```
ViStatus PXI3072_XilinxDownload(ViUInt32 Card, ViChar *FileName);
```

Parameters:

card

Index of the PXI/ PCI 3072 board, beginning left with 1

Pointer, for example FileName, to the path of the FPGA file to be loaded

Description:

The GPxi3072_XilinxDownload function allows to load an FPGA file (**.cfd* extension) to the XILINX. This file serves, among other possibilities, to read the geographical slot address in the PXI rack.

The loaded data is volatile. Therefore the function has to be executed again after switching off power.

After XilinxDownload, a delay of about 500 ms is required (as all controllers execute a power-on reset).
Then, carry out the 0x10 Software Reset firmware command for all controllers to come into the normal operating mode from bootloader mode.

3.2.2.5 XILINX Write Data

The PXI3072_XilinxWriteData function allows the configuration and execution of functions provided by the XILINX.

Format:

```
ViStatus PXI3072_XilinxWriteData(ViUInt8 WriteData[]);
```

Parameter:

Pointer, for example WriteData ,to the Write data area
(currently max. 128 bytes per command)

Description:

Before using the functionality of the XILINX, the corresponding FPGA file must have been loaded by PXI3072_XilinxDownload
(see XILINX Download).

The data format consists of four bytes including the command.
If necessary parameter bytes can follow.

Data format:
- 1st byte: 0x48 (StartByte)
- 2nd byte: card (index of the PXI/ PCI 3072 board, beginning left with 1)
- 3rd byte: 0x00 (Reserved byte)
- 4th byte: XILINX command

Currently supported XILINX command:

0x10 PowerOnReset for the complete board

3.2.2.6 Write Data

The PXI3072_WriteData function is for writing data to the selected controller.

Format:

```
ViStatus PXI3072_WriteData(ViUInt8 WriteData[], ViUInt32 Length_In_Bytes);
```

Parameters:

Pointer, for example WriteData, to the Write data area, consisting of Command Header and Command Bytes (currently max. 1024 bytes per command)

Length_In_Bytes

Size of the memory area WriteData is pointing to, in bytes

Description:

The PXI3072_WriteData function allows writing of data to the selected controller.

In the header of the structure WriteData is pointing to, there is the information regarding the PXI/ PCI 3072 board and the controller to be activated by this function.
Therefore these parameters are not to be given separately.

3.2.2.7 Read Data

The PXI3072_ReadData function is for reading data from the selected controller.

Format:

```
ViStatus PXI3072_ReadData(ViUInt32 Card, ViUInt32 Port,
                          ViUInt8 ReadData[], ViUInt32 *Length);
```

Parameters:

Card

Index of the PXI/ PCI 3072 board, beginning left with 1

Port

Number of the controller (1..3)

Pointer, for example ReadData, to the Read data area, consisting of Response Header and Response Bytes (currently max. 1024 bytes per response)

Length

Value of the parameter before function call:
Size of the buffer pointed by ReadData in bytes

Value of the parameter after function call:
Number of bytes actually read

Description:

The PXI3072_ReadData function allows reading of data provided by a controller
(see also GPxi3072_DpramReadResponse in the Windows Device Driver section).

3.2.2.8 Reset Port

The PXI3072_ResetPort function is for releasing a software reset for the selected controller.

Format

```
ViStatus PXI3072_ResetPort(ViUInt32 Card, ViUInt32 Port);
```

Parameters:

Card

Index of the PXI/ PCI 3072 board, beginning left with 1

Port

Number of the controller (1..3)

Description:

The PXI3072_ResetPort function releases a software reset for the selected controller of a PXI/ PCI 3072 board.

This releasing procedure is executed via a separate interrupt channel, NOT via the command interpreter of the software (0x10 Software Reset firmware command).

3.3 Programming with LabVIEW

3.3.1 LabVIEW via G-API

The supplied CD contains VIs for activating PXI/ PCI 3072 boards under LabVIEW.

The functions of GOEPEL's G-API are used for this.

3.3.2 LLB using the Windows Device Driver

The supplied CD contains VIs for activating PXI/ PCI 3072 boards under LabVIEW.

The functions described in the Windows Device Driver section are used for this.

3.3.3 LLB using the VISA Device Driver

The supplied CD contains VIs for activating PXI/ PCI 3072 boards under LabVIEW.

The functions described in the VISA Device Driver section are used for this.

3.4 Further GOEPEL Software

PROGRESS, Program Generator and myCAR of GOEPEL electronic GmbH are comfortable software programs for testing with GOEPEL hardware.

Please refer to the corresponding User Manual to get more information regarding these programs.