Single Boundary Scan IC looking for connection

Boundary Scan according to IEEE1149.x has evolved over the last 10 years to become a technology used in an increasingly broad spectrum of applications for embedded testing of complex electronic units. BGA/CSP components in particular are fuelling this trend. However, Boundary Scan is not integrated in all ICs, a fact that often leads to controversial discussions regarding the question of the test coverage achieved in applications with a low Boundary Scan portion. The following article highlights the integration of Boundary Scan from a technical testing perspective, analyses the variety of options for increasing the fault coverage and shows how this potential can be exploited in practice using the latest system solutions.

Four pins define the difference

In contrast to traditional ICs, IEEE1149.x compatible ICs have four (five with optional test reset) extra pins, often also called JTAG pins. A so-called Test Access Port (TAP) is connected to these pins, forming the serial interface for on-chip registers and can be cascaded across multiple chips as shown in Figure 1. For more details on how this works, please see the literature [1].

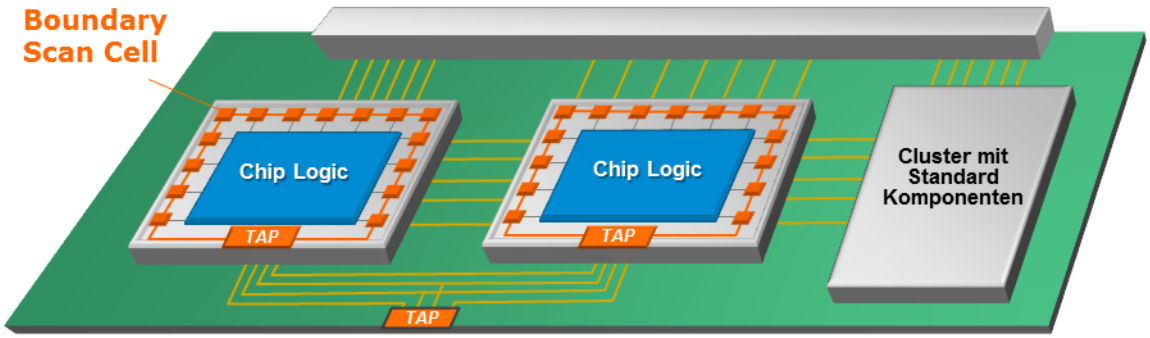

Figure 1: Schematic Boundary Scan architecture on a board

One of the registers controlled by the TAP is the Boundary Scan Register (BSR), which consists of Boundary Scan cells. Typically, a cell such as this is located at each signal pin on an IC. This implementation results in a hierarchical three-way split of the structural design of a chip (Figure 2) and thus also of the electronics unit associated with the chip. In so-called Test Mode, the Boundary Scan electronics actually move in an isolating manner between the on-chip functions and the connecting structures contained on the printed circuit board. In Mission Mode, however, Boundary Scan is switched transparently, connecting the chip logic to the signal pins as in a standard IC.

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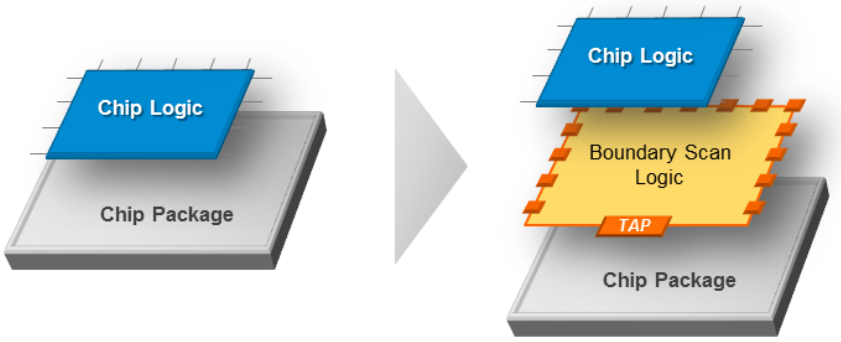

Figure 2: Expansion of the structural levels with Boundary Scan

On account of this isolation, the Boundary Scan logic can be operated completely independently of the chip logic and can focus purely on testing the connections connected to the chips. This brilliant separation of structure and function is the real key to the efficiency of the Boundary Scan process. The isolation of the chip logic is carried out by multiplexers in the Boundary Scan output cells, while the input pins are typically simply contacted in parallel (Figure 3). In practice, there are a variety of extremely different Boundary Scan cells, which are integrated tailored to the type of signal pin and the desired function.

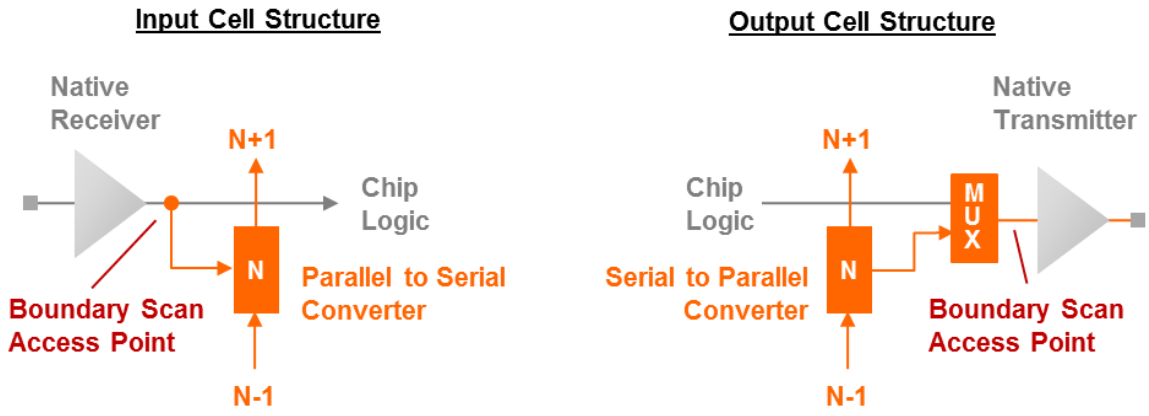

Figure 3: Simplified access schematic in Boundary Scan cells (example)

From a technical testing perspective, the previous explanations reveal a series of remarkable facts:

- Boundary Scan uses the chip's native drivers/receivers to detect any interface faults directly. It therefore “sees” what the silicon sees.
- Boundary Scan moves the pin electronics of a tester directly into the silicon of a chip, with the Boundary Scan cells constituting the tester logic, which is controlled by serial command via

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the 4-pin bus. However, the test functionality and flexibility of these pin electronics are not comparable with an external tester (e.g. ICT) with programmable levels, timings, etc.

- Although the Boundary Scan standard defines various types of Boundary Scan cells, it does not stipulate that any such cell must be present at every pin. In plain terms that means that even Boundary Scan ICs can have thoroughly conventional pins. The decision lies with the chip designer (virtually making him a test engineer).
- Boundary Scan is a technique which uses on-chip electronics to get testing access to the pins, but this does not automatically define the associated test strategy in the sense of "the" one and only Boundary Scan test.

The last statement in particular will be explained in more detail below, because in practice Boundary Scan focuses on the highly complex BGA modules such as FPGAs, processors and ASIC. This is understandable from a cost point of view, too, and will not change in perspective. As a result, in many applications often only a Boundary Scan IC is included, which is "surrounded" by non-scan memories, mixed-signal circuits, bus components, flash or connectors to name but a few. Often in such cases, the hopelessness of the Boundary Scan is foreseen and bizarre fault coverages in the region of 0% are postulated. But is that really correct?

One swallow does make a summer

A systematic analysis of possible circuit scenarios using 3-level model introduced in figure 2 results in a fundamental partitioning in the form of a "Unit Under Boundary Scan Test" (Figure 4).

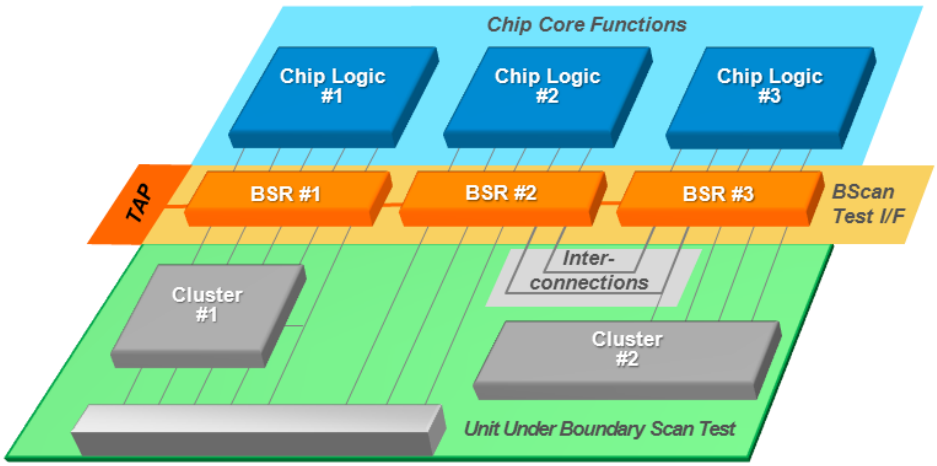

Figure 4: Schematic structural partitioning of a Unit Under Boundary Scan Test

For the purpose of simplification, serial daisy-chaining of all Boundary Scan Registers (BSR) is assumed here, with the result that all Boundary Scan cells operate synchronously in EXTEST mode.

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Proceeding from the Boundary Scan test interface, a number of relevant test procedures emerge (Table 1).

Test type	Aim	ATPG	AFD
Infrastructure	- Testing of all TAP connections - Testing of on-chip registers - Testing of the chip ID	√	√
Interconnections	- Testing of the BScan pin-to-pin connections - Testing of BScan pin-to-pin bus connections - Testing of pull/up and pull down	√	√
Clusters	- Testing of the connections to clusters - Testing of the non-scan cluster components - Testing of in-line resistors, buffers	(√)	(√)

Table 1: Classification of important Boundary Scan test procedures

Each of these test procedures is aimed at completely covering certain elements. Whereas the infrastructure test is more or less a kind of self-test of the Boundary Scan tester, the interconnection test scrutinises the functionality of single and bus connections between BScan pins. For both procedures, high-quality support tools exist in the form of automatic test program generators (ATPG) and for automatic fault diagnosis (AFD) at the pin level. It is in the nature and history of the Boundary Scan process that the interconnection test in particular is often included as a single procedure in the analysis of testability – and herein lies the problem: the Boundary Scan test logic only defines access points. The way in which these are used is covered on a completely different sheet.
In this way, the non-scan components connected to BScan pins can also be covered by so-called cluster tests, and in practice there exists a wide variety of different cluster types. If this option is admitted in the analysis of fault coverage for modules with, for example, only a BScan IC externally, the disaster is preprogrammed in the ranking with other test methods. But how do cluster tests such as these actually work and – most importantly – to what extent can they be controlled in practice?

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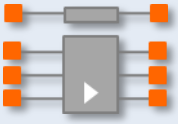
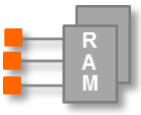
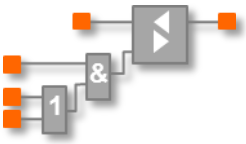
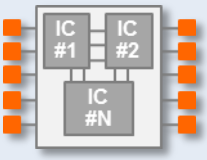
Living on the edge with the cluster test

The clusters are the real crux and stumbling block in the discussion of fault coverage, because at first glance controlling them seems to be critical. Appropriate attention must therefore be given to this problem area.
In principle, the following types of clusters can be distinguished:

- Transparent clusters (in-line resistors or buffers between BScan pins)
- Storage clusters (sRAM/dRAM modules on BScan pins)
- Device clusters (single ICs or sensors/actuators connected to BScan pins)
- Logic control clusters (control logic with one or more basic gates)
- Glue logic clusters (more complex multi-device clusters)

A cluster here can in principle be considered a function complex, which must also typically be used to apply a function test (Table 2).

Cluster type	Circuit structure	Test generation	Fault diagnosis	Comment
Transparent cluster		- ATPG as part of the interconnection test	- Pin level - Network level - Opens/shorts	Support for multiple cascaded buffers also possible
Storage cluster		- RAM ATPG	- Pin level - Network level - Opens/shorts	Only connection testing of the pins and networks, not a complete test of the memory cells
Device cluster		- Device ATPG - Truth table ATPG - Manual scripting - Waveform editing	- Pin level - Network level	Can be used for digital ICs, mixed-signal ICs, actuators and sensors
Logic control clusters		- ATPG as part of the interconnection test	- Pin level - Network level	Automatic generation of the control pattern
Glue logic cluster		- Truth table ATPG - Manual scripting - Waveform	- (Pin level) - Network level	Effort required for test creation and troubleshooting very high

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	editing - ATPG IEEE1445

Table 2: Overview of the individual cluster situations.

Control of all these manifestations is of course only possible when appropriately powerful and sophisticated tools are available for test development. An example of this is the JTAG/Boundary Scan software platform SYSTEM CASCON™ from GÖPEL electronic [2]. The support here ranges from identifying the respective clusters and generating test programs to fault diagnosis and the display of fault locations in the layout. The clusters are in many cases handled automatically and in some cases also in combination with other procedures.
This applies on the one hand to the transparent clusters, but also to the logic control clusters, which are both an integral part of the interconnection tests. The advantage of this method lies in the higher fault coverage, because all structures are activated in parallel. The physical cause of the fault can in most cases be localised in most cases be pinpointed immediately in the form of shorts or open pins.
In the case of storage clusters, the test focuses on the connections between the BScan pins and the memories. Special structural algorithms are used for this, which perform read and write operations on selected memory cells and compare the vectors. As a result, the physical faults can in many cases be diagnosed immediately here, too. The definition of the read and write operations is stored in the IC library in the IC model of the memory and is processed by the ATPG. This makes continuous modifications of the model depending on the application unnecessary.
In practice, one of the most important applications is the testing of a device cluster. This can be active components (IC, LED, actuators, sensors, etc.) or passive parts (e.g. switch). There is a wide variety of possibilities for test coverage. They range from the definition of a truth table with incremental stimuli and response vectors and editing of waveforms right through to manual scripting of the test program.

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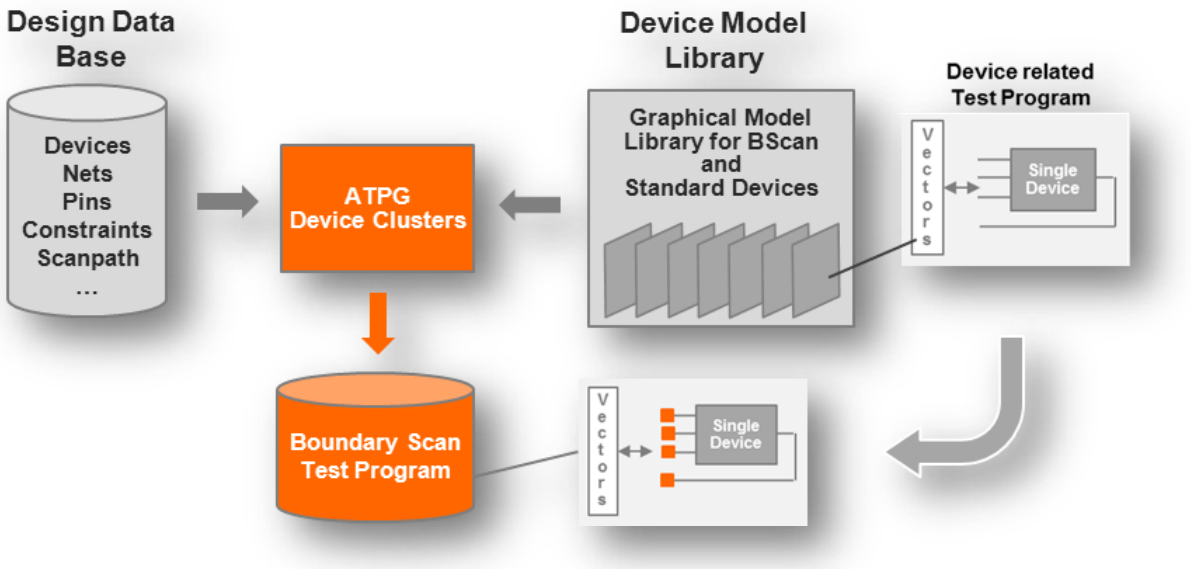

Figure 5: Schematic of the automatic test program generation in device cluster tests

A particularly efficient variant, however, is the use of the so-called device ATPG. In this method, test models are stored in the graphical model library for the non-scan components, and these test models are then automatically linked to the respective Boundary Scan pins during ATPG (Figure 5).
The tests of individual components are stored as source code in the specific JTAG/Boundary Scan language CASLAN™. The models are an integral part of the library, but any missing models can also easily be maintained or adapted by the user or by the system supplier. The graphical model library consistently contains all the structural and functional information for all BScans and standard ICs and thus plays a key role in the work of the whole system.

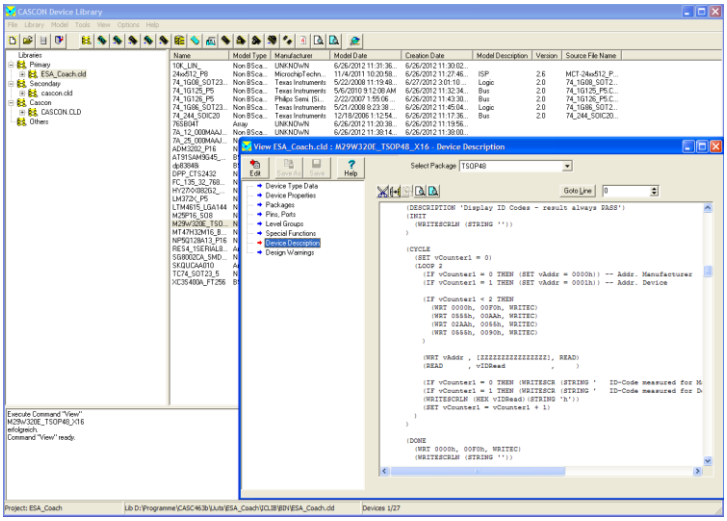

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Figure 6: GUI of the graphical model library of SYSTEM CASCON™

The programs produced as a result of the ATPG are also in CASLAN source code and can therefore easily be debugged and adapted, too.

The last cluster category is the glue logic clusters. They cover several ICs and reflect complex functions. The testing of such constructs is associated with a high level of effort and must typically be generated manually. SYSTEM CASCON still offers alternative ways of adopting test vectors in the DTIF format (IEEE1445), but in order for this to be possible appropriate simulations must have been carried out in the EDA environment.
In practice, however, clusters such as these are interestingly relatively rare on complex boards since, for reasons of packing density, such function clusters are preferably integrated in the PLD/FPGA, which in turn of course miraculously provide a Boundary Scan.

As a final point on the subject of cluster testing, it must be noted that all tests are static, which means that they are able to find absolutely no dynamic faults. They are, however, perfectly suited to covering typical production faults.
In spite of all the techniques shown, testing gaps nonetheless remain, such as open connections through connectors, peripheral clusters with external I/F, or analogue components. So is this the end for BScan, or are there other options for such cases?

Charming test technology seeks partnership

One of the advantages of the Boundary Scan is its flexibility when it comes to open expandability in hardware and software. It comes as no surprise, then, that there are in fact several variants to solve the problems addressed elegantly:

- organic expansion of the technology through external boundary-scan hardware
- combination of Boundary Scan with other electrical test processes
- mixed use of Boundary Scan with AXOI systems

When using an external Boundary Scan I/O module, the entire process is natively expanded (figure). The entire process flow in principle remains unchanged, and only the additional hardware is docked to the target design for the software.

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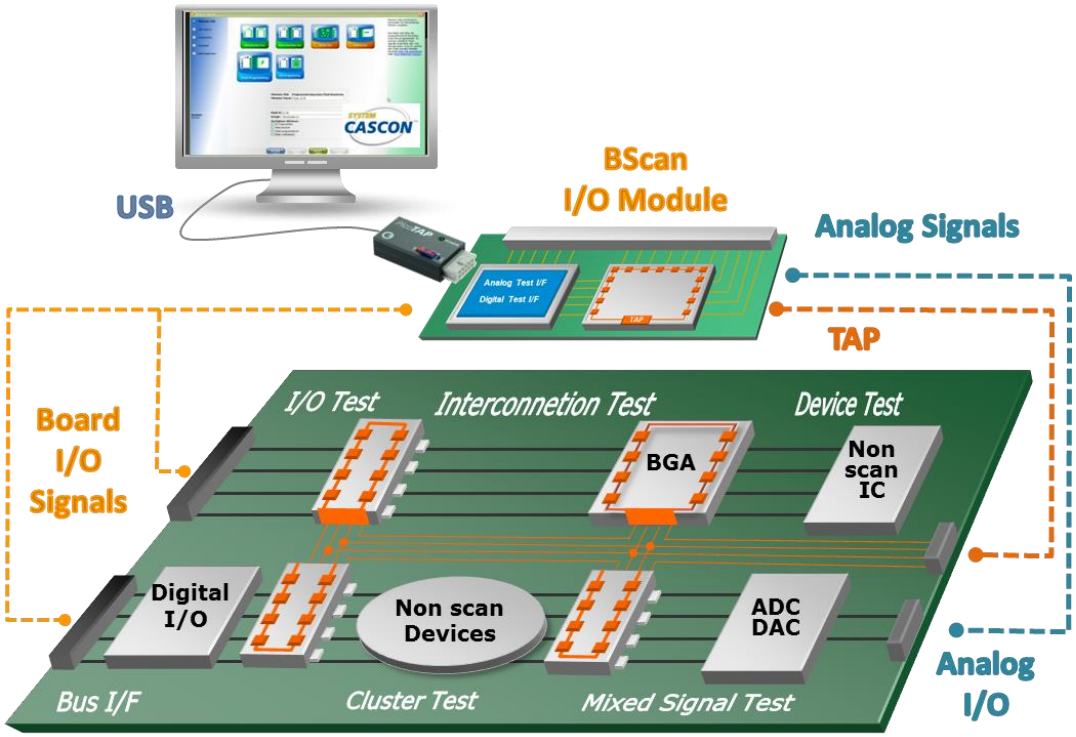

Figure 7: Example of the use of a Boundary Scan module for expanded test coverage

Modern Boundary Scan modules are also equipped with other additional digital and analogue resources, and as a result the fault coverage as a whole can be considerably expanded. Leading the way here is the CION-LX I/O module, which provides support based on a special tester on chip (ToC) ASIC [3] IEEE1149.x standard and has various additional analogue and digital resources for each pin, which can be controlled statically and dynamically. This means that at-speed tests can also be realised.

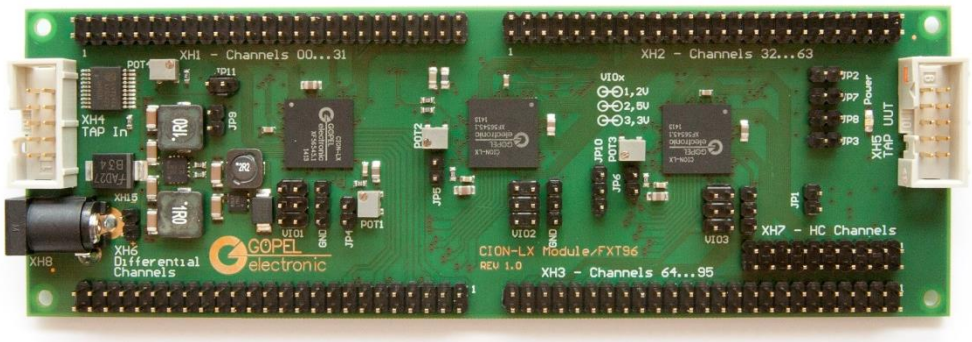

Figure 8: Multifunctional mixed-signal I/O module CION-LX/FXT96 with TAP cascading

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Although Boundary Scan was actually developed as a removal concept for the use of physical needles, the I/O channels of a module such as this can of course very easily be applied to the unit under test via needles. This is still a common scenario in production in order to contact the periphery, for example, or to check voltages in the circuit. Equally, it is also possible to contact test points in the circuit (if there are any) in order to increase test coverage further. For some years now, ready-made JTAG/Boundary Scan testers have in practice also been available, with integrated I/O modules, power supply, replaceable needle cassette, etc. (Figure 9).

Figure 9: Complete JTAG/Boundary Scan Tester JULIET™

Another way of additionally improving the test coverage is to combine Boundary Scan with other electrical test methods such as an In-Circuit Test (ICT), Flying Probe Test (FPT), or Functional Test (FCT). The hardware and software components must be integrated in the respective tester platform here. However, only a real interaction between Boundary Scan and the tester channels can achieve the added value of increased fault coverage. As one of the pioneers of integration solutions, GÖPEL electronic introduced the Virtual ScanPin™ method more than 15 years ago (Figure 10).

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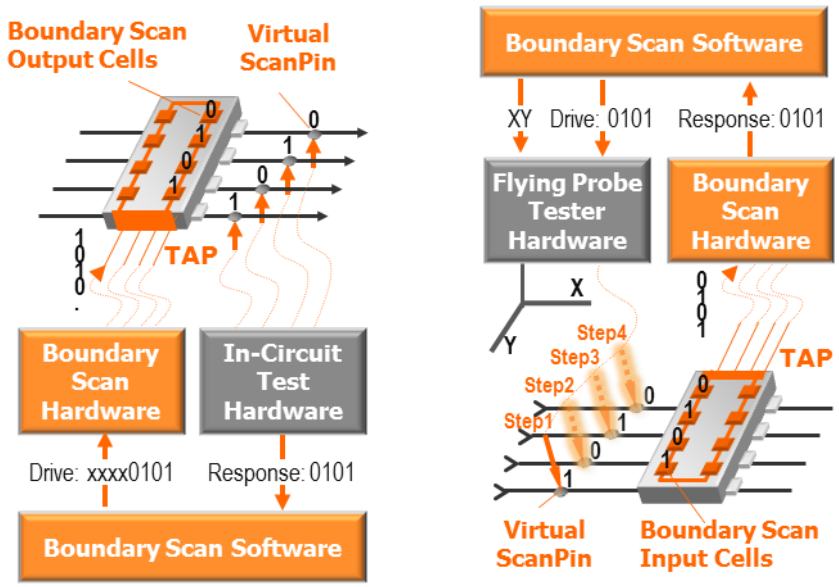

Figure 10: Schematic showing the use of ICT/FPT tester channels as Virtual ScanPins

The process is completely automated by sophisticated ATPG tools and is available for all leading tester platforms in the form of integration packages. This also applies to the function test, where modular instrumentation platforms such as PXI™ or PXIe™, for example, are increasingly widely used. In this case, the test channels are provided by PXI I/O modules (Figure 11).

Figure 11: Boundary Scan controller and I/O module with 96 channels for PXI/PXIe

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The last of the three possibilities mentioned above is to mix a Boundary Scan Test with Automated X-Ray/AOI (AXOI) systems. This is not a physical combination, however, but a fusion of electrical fault information and inspection data. As a result, the quality of the solder joints of scan-enabled and non-scan BGA pins can be precisely measured according to IPC-A-610E, for example, and used to control the process parameters [4].

Summary and conclusions

Even if only a few – or, in extreme cases, only one – Boundary-Scan-enabled ICs are present on the unit under test, the attainable test coverage should nevertheless be analysed thoroughly using cluster tests. Modern Boundary Scan test systems offer a wide range of diverse software tools for this with a high degree of automation and very good diagnostic quality. Furthermore, by using external I/O modules, the test coverage can be hugely extended in an organic manner, both simply and cost-effectively. Combination with other tester platforms is also an attractive alternative for using available resources for extended Boundary Scan testing. For both approaches, there is a wide range of sophisticated system solutions with ready-made functionality. Moreover, the efficiency of the Boundary Scan can further be increased by the strategy of Embedded System Access [5] developed by GÖPEL electronic.
Ultimately, there are many ways of facilitating appropriate connections with single BScan ICs – what is crucial, however, is the planning of the test strategy and also the will to exploit the potential shown.

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