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# Overcoming the limitations of JTAG/Boundary Scan

Electronic components and assemblies are becoming increasingly complex. The requirements for test equipment are also changing rapidly. For a long time, intrusive test procedures, such as the in-circuit test (ICT), have been the benchmark. However, these processes reach their limits, especially with decreasing component and assembly sizes and simultaneously increasing component densities. Due to the continuously reduced test access, the test electronics were increasingly shifted to the circuit to be tested. With the introduction of Boundary Scan technology (IEEE Std. 1149.X) and the JTAG interface in 1990, access was created that uses pin electronics integrated into the chip for testing. This non-intrusive process still forms the basis of a wide range of access options for debugging, testing and programming.

But even the classic Boundary Scan test cannot always meet all requirements. The limits of a serial shift register become apparent, especially when considering the access and test speed. GÖPEL electronic has been (further) developing new technologies for 30 years. These technologies are based on the IEEE 1149.X standard, but sometimes far exceed its performance. All these technologies and their applications are combined under the term "Embedded JTAG solutions". But what advantage do these technologies offer over the standard Boundary Scan? When is this no longer sufficient and which requirements can be best implemented and how? The following article provides an overview of all test requirements and the appropriate test strategies.

## The 3 pillars as a framework

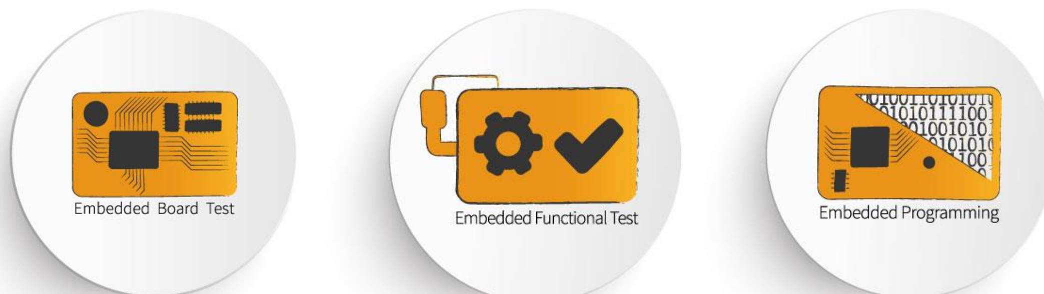


*Figure 1: The three pillars of Embedded JTAG Solutions*

In order to facilitate classification, it is helpful to illustrate the various areas of technology and application as pillars. Depending on their application, they are called Embedded Board Test, Embedded Functional Test and Embedded Programming. These three pillars describe specific application scenar-


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ios that users encounter on a daily basis in electronics development or production. Short application examples of the three pillars are described in more detail below.

The basic approach of the *Embedded Board Test* is to verify flawless connections on the unit under test. In this way, it is possible to diagnose short circuits, non-soldered pins, or even missing pull resistors. However, this type of access has even greater potential: The technology can also be used to conduct RAM connectivity tests. In doing so, all address, data and control lines are addressed with defined test patterns. With the help of these test patterns, pin-accurate error statements can be made regarding the correct connection between the controller and the RAM device. Connections to external FLASH modules or elements with serial interfaces (e.g. $I^2C$, SPI, MIDO, …) can also be tested. Likewise, all address, data, and control lines are addressed— to read out and evaluate the device and manufacturer ID, for example. In this way, correct circuit component placement and connections are verified. Modern assemblies utilise a wide variety of interfaces. Here, for example, digital as well as analogue IOs and functional interfaces (e.g. CAN, Ethernet or USB) CAN be tested using simple adaptations.

*Figure 2: Starter set for simple JTAG/boundary scan applications: SCANBOOSTER II Designer Studio*

However, today's test strategies now require more than simply checking board connections. In addition to ensuring flawless contact, the board and component function in particular must also be checked. These test requirements and the associated strategies are combined under the designation *Embedded Functional Test*. In this way, various on-board instruments can be addressed and evaluated. Position and temperature sensors, ADCs, DACs, and a wide range of transceivers are equipped with standardised configuration interfaces (e.g. $I^2C$ or SPI). Simple read and write access can be used to check the correct functioning of these modules. On-chip instruments and interfaces can also be func-

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tionally checked. The resources on the board are used, for example, to initiate and review USB host/slave communication.

With the characteristics of the JTAG/Boundary Scan process, the Boundary Scan output cells can also be used to program memories in development and production. However, this programming is comparatively slow due to the path through the scanning chain. Increasing file sizes and growing demands on programming speed represent particularly significant hurdles.
New technologies have created new ways of doing this. All options are summarised under *Embedded Programming*. From programming serial numbers and production data to loading entire firmware packages, there are extremely different data throughput requirements. JTAG/Boundary Scans can be used when only small quantities of data are programmed, or when there are no special requirements regarding test duration. For larger quantities of data or shorter test durations, alternative access technologies (e.g. so-called VarioTAP for processor emulation) can be used. Since these methods do not use serial shift registers for data transfer, they can achieve significantly higher programming speeds. The selection of the correct EJS technology therefore depends entirely on the required programming speed and the element to be programmed.

## Testing at every level

In addition to the vertical division of the application fields (as described above), a distinction can be made from an application perspective between three levels in terms of speeds.
The lower *Standard* level is defined by the static test. This default access refers to the known boundary scan test options. The test speed is therefore far below the actual board function. Classic connection tests in particular take place at this level. However, at this access level, it is also possible to address external modules, e.g. to read out a component ID to verify correct assembly. Only low programming speeds (Bytes/s to a few kBytes/s) are achieved in the *Embedded Programming* area.

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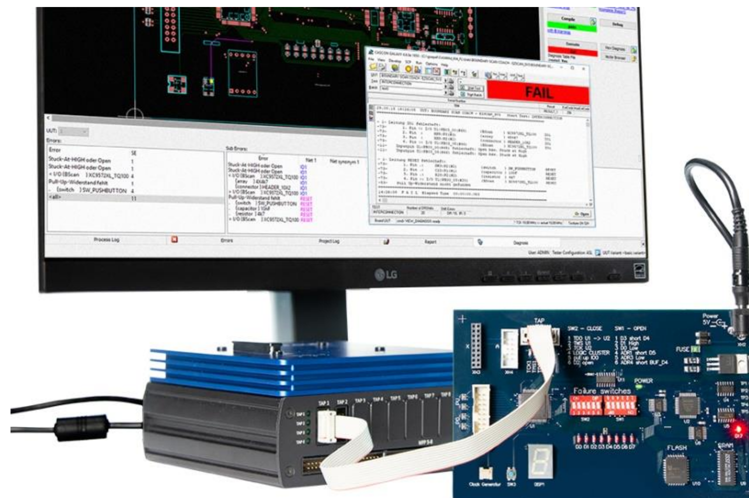


*Figure 3: Embedded JTAG Solutions Controller "SCANFLEX II" in operation with SYSTEM CASCON software*

Higher access speeds are already achieved in *the Boundary Scan Plus* level. The matrix classifies the test speed as *an at-speed*. Although the test speed is still below the actual board function, it is significantly faster than the conventional Boundary Scan test, so we no longer assume static signals. Basically, the test speed is now defined by debug access. For example, a RAM connection test in *the Boundary Scan Plus* level can also diagnose dynamic problems with termination resistors. Significantly higher speeds can also be achieved during programming by using VarioTAP or ChipVORX technology (kBytes/s).

*Figure 4: ChipVORX module for testing high-speed interfaces*

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The highest speeds are achieved in the highest *IP Plus* level. We are now talking about the nominal or stress level test. The nominal speed is tested with the speed of the final board function. If the test speed exceeds the board function normally intended, this is referred to as the stress level test. The final specification will therefore even be exceeded. A typical application is, for example, a Bit Error Rate Test (BERT) on high-speed interfaces. During programming, high speeds are achieved in the *IP Plus Level* (MBytes/s), in which programming data can also be transmitted via communication interfaces (e.g. Ethernet).

The three vertical pillars and horizontal power planes shown combine to form a matrix called the Boundary Scan Plus Matrix. It provides an overall overview of the Embedded JTAG Solutions and their applications.

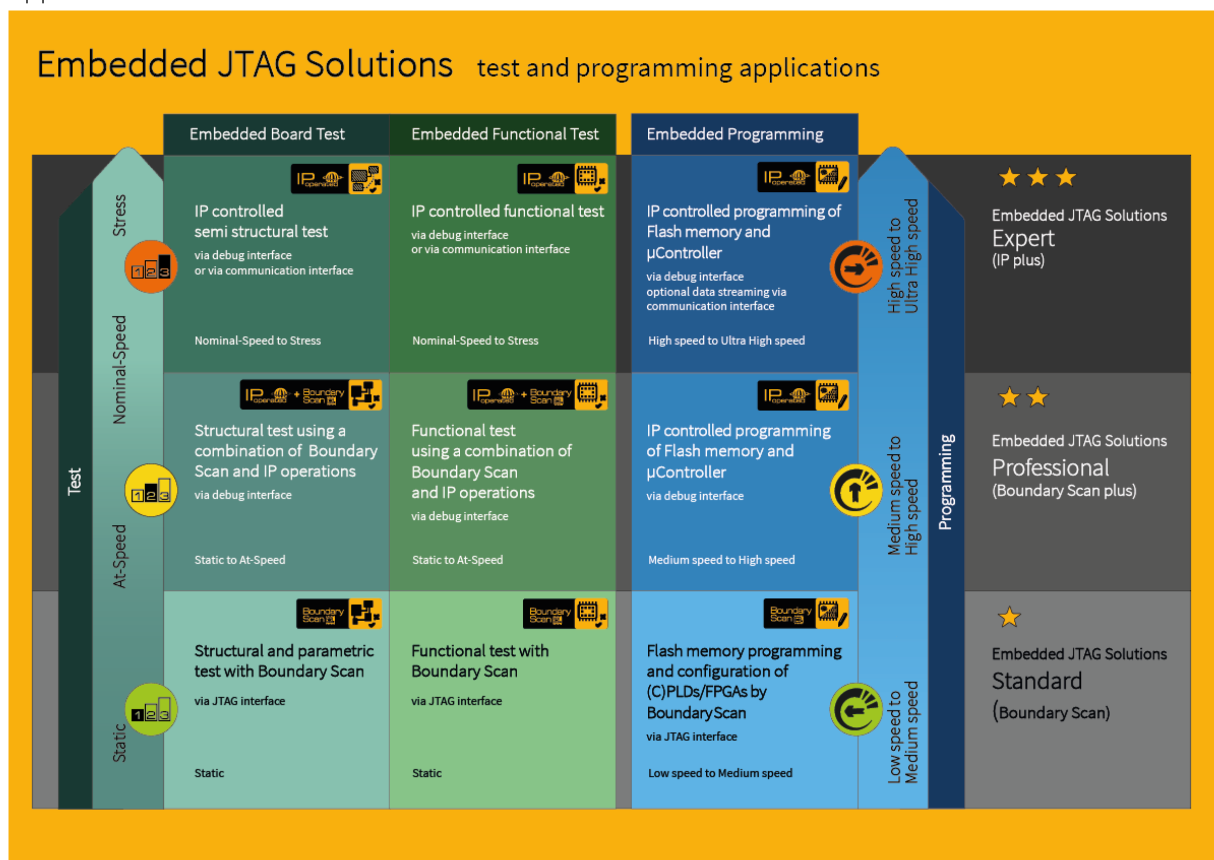


*Figure 5: Boundary Scan Plus Matrix*

## Solutions in every field

The three application areas and three access levels of EJS technologies result in a total of nine application fields. There are very specific requirements and solutions behind each field. An accurate analysis of the unit under test and the test specification can be used initially to clearly define the areas in

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which the test system must be designed. This classification ultimately simplifies the selection of the correct test equipment and the selection of test routines to be performed. The Boundary Scan Plus Matrix thus provides an ideal overview for all EJS technologies that now offer far more than just simple JTAG access.

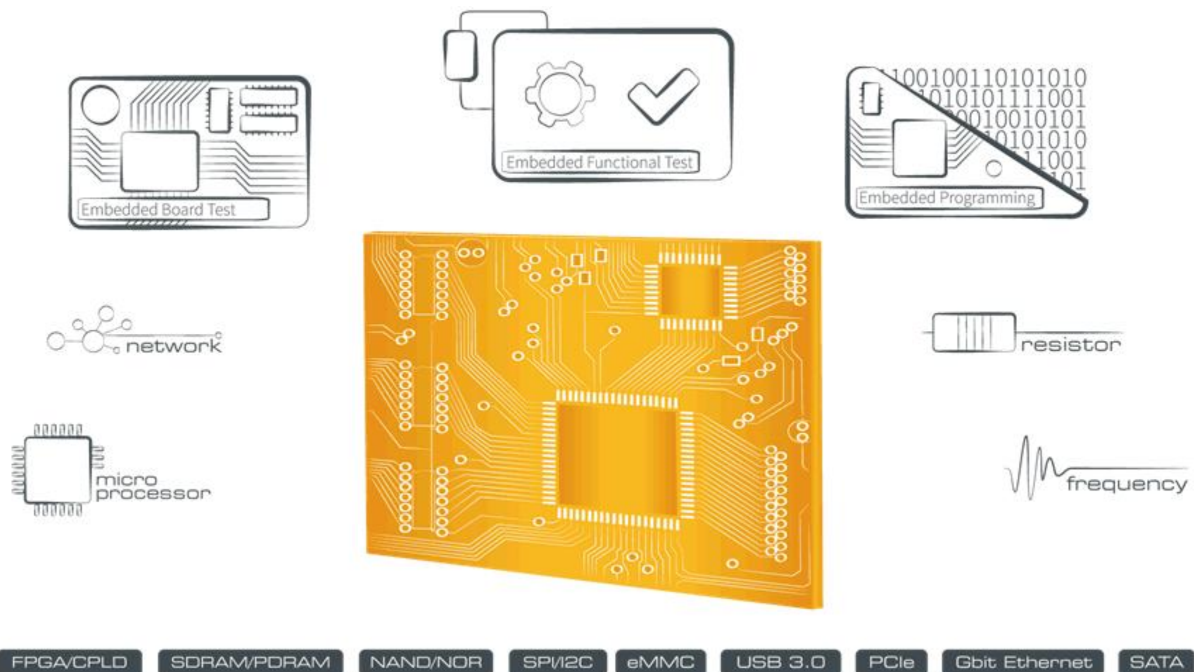


*Figure 6: Example depiction of application possibilities within the embedded JTAG solutions and Boundary Scan Plus Matrix*

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