Automatic board test made by FPGA

Thanks to their flexibility and constant performance improvements, Field Programmable Gate Arrays (FPGA) are increasingly being used in the design of modern system solutions. The latest developments with multi-core features and high-performance GBit interfaces are fuelling this trend with lasting effects. From a testing perspective, however, FPGAs offer far more possibilities than simply realising an application. For example, they can also be transformed into design-embedded test centres for validating prototypes or for tracking down the fault fiend in production testing. In order to fully exploit the potential of test strategies such as these, however, correspondingly powerful tools are necessary for continuous process automation.

Good test prospects thanks to FPGA-embedded instruments

The increasing complexity and speed of modern electronics units is leading to ever-increasing problems when it comes to testability. In particular, erosive mechanical test access is increasingly causing problems when using conventional test and measurement devices. The use of chip-embedded instruments offers a way out of this dilemma, and according to Figure 1, there seems to be a particular focus on FPGA-based instruments at this point.
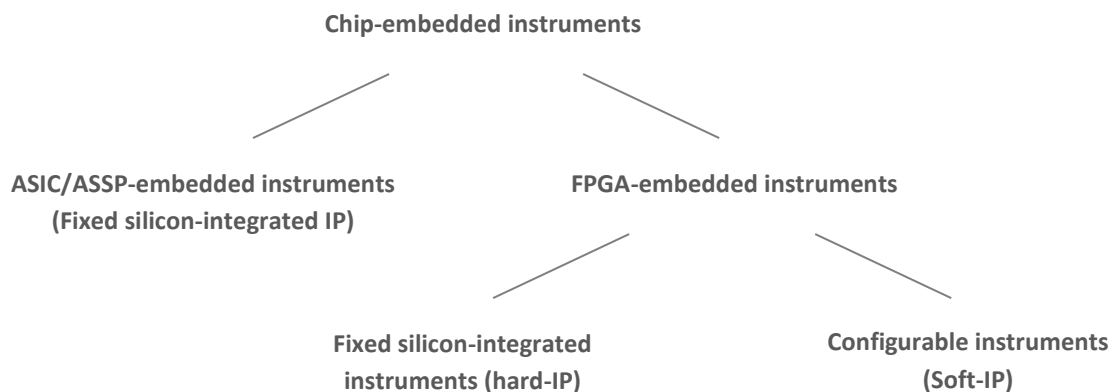
Chip-embedded instruments

**ASIC/ASSP-embedded instruments
(Fixed silicon-integrated IP)**

FPGA-embedded instruments

**Fixed silicon-integrated
instruments (hard-IP)**

**Configurable instruments
(Soft-IP)**

Figure 1: Classification of embedded instruments

Unlike external devices, embedded instruments are directly integrated in the native circuit environment at chip level This solves the main problem of mechanical access in a very elegant way. This eliminates the need for painstaking invasive probing of fine pitch connections or conductor tracks. In addition, there are a series of further important advantages and disadvantages which arise in this context, however:

- The instrument sees the real intrinsic signal in silicon
- Signal distortions are ruled out thanks to mechanical sampling
- Instrument and test target are firmly connected
- The performance of the instrument is linked to the parameters of the silicon
- The extent to which the power of an embedded instrument can be defined is limited
- Embedded instruments are generally optimised for a specific application
- In embedded instruments, there is no parametric analogue qualification of input signals on account of the digital receiver which is typically present

It is clear that embedded instruments never come close to achieving the flexibility and the universal, target-independent analysis capabilities of a stand-alone unit, but can perform a specific task efficiently, a certain task efficiently and with a high level of performance and precision.

The integration of instruments in silicon as functional IPs (intellectual property) is fundamentally nothing new and is practised as standard as an important element in chip testing for a long time. There is a broad range of BIST-IP (Built-In Self-Test) here for all possible applications, such as PLL-BIST, Logic-BIST, Memory-BIST etc. The use of these instruments for board testing is by contrast still incredibly recent. The natural separation of chip and board development complicates matters here. As a result, chip developers are in some cases far from fully aware of the needs and desires of board developers, or these needs and desires are too expensive to implement and in some circumstances completely infeasible with the required range of functions, however. In this connection, the standard IEEE1149.1 (JTAG/boundary scan) [1] was a ground-breaking innovation, which saw specific chip features introduced for the board test for the first time. More recent standards such as IEEE1687 [2] will reinforce this trend.

Seen in the context of this overall situation, FPGAs are a real boon for test engineers. Their programmability largely nullifies the reliance on prescribed instrument IPs. According to Figure 1, this enables transformation of design-integrated FPGAs in embedded multi-functional test centres with configurable instruments.
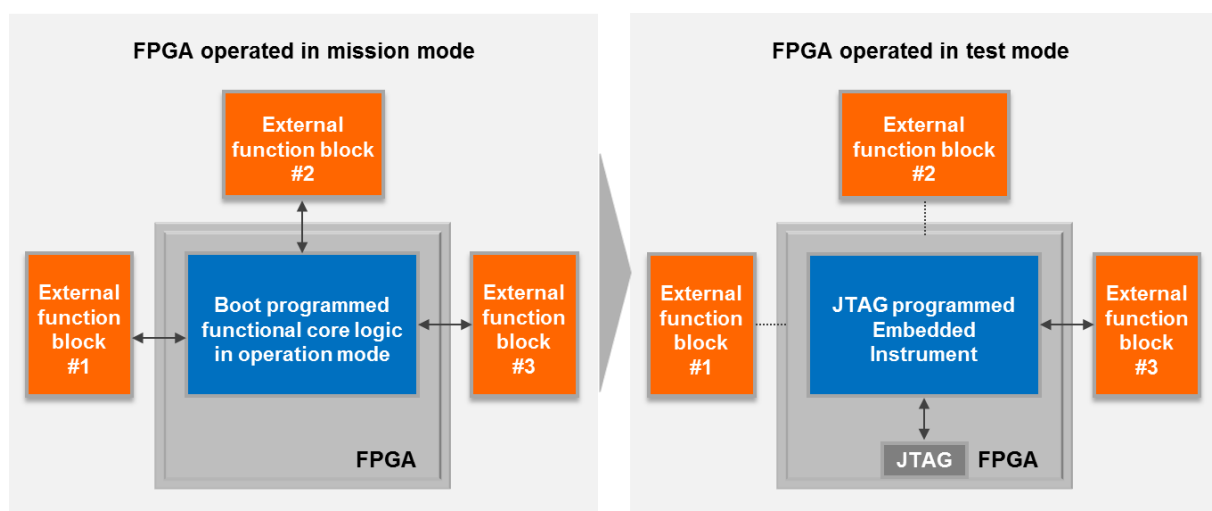
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Figure 2: Example of the use of an embedded instrument in test mode

The FPGA is programmed using the standard JTAG-TAP (Test Access Port), which is also used for boundary scanning. Thanks to this synergy, no additional infrastructure is necessary on the board. At the same time, the JTAG port also serves as a control medium for the instrument-IP, since all leading FPGA providers enable mapping of custom designs onto the JTAG registry structure as standard.

Whereas a quick GO/NOGO assertion is often sufficient as a test result in the chip test, the situation is completely different for the board test. Here, the repair information requested is typically a detailed pin-level fault diagnosis. In this sense, the IP requirements relating to functionality, controllability and test data throughput are subject to different criteria and the overall process becomes more complex. It is possible to distinguish between three phases, according to Figure 3.
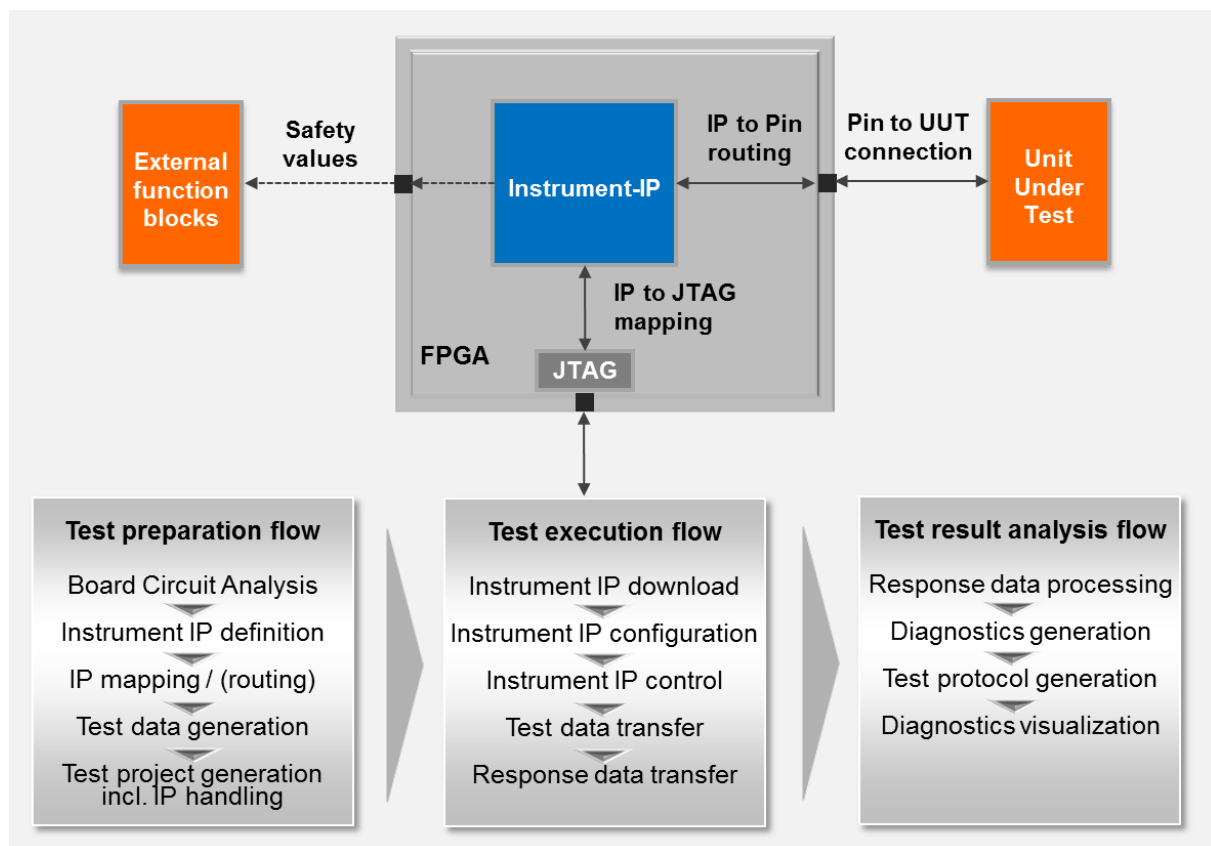

Figure 3: Typical process flow when using FPGA-embedded instruments

The testing equipment and the test program are effectively specified in the project preparation phase. This step must be specifically focused on the needs of the Unit Under Test (UUT), but guarding of the

remaining circuitry connected to the FPGA and of the board as a whole must also be ensured. If this is not the case, an undefined status could affect the test, or in extreme cases even result in destruction. The test is executed in the second step. This includes initialisation of the entire instrument-IP, as well as applying the guarding level.

The third step is the analysis of the test results, including diagnosis generation and error visualisation. Depending on the nature and objective of the test, the process flow may also vary slightly. This depends on the one hand on the desired diagnostic depth, but the test equipment used and the overall strategy chosen for realising the FPGA-embedded instrument also play a role.

Automation makes the difference

While the use of FPGA-embedded instruments appears at first glance to be relatively trivial and straight-forward, more detailed analysis, as shown in Figure 3, leads to a whole variety of influencing factors and fundamental decisions. The most important of these are:

- How is the FPGA-to-UUT topology detected?
- Who provides the instrument-IP?
- How is JTAG mapping performed?
- How is IP-to-pin configuration carried out?
- How is the IP control implemented?
- Who generates the test data and the guarding vectors?
- How is the overall project creation carried out?
- How is diagnosis performed?
- How much time is required for the entire project creation process?
- What FPGA design skills and tools are needed?

The range of responses may be very large in practice and will also include serious differences in the expenses incurred. From the perspective of automation, however, we can divide these broadly into three categories, according to Table 1.

Influencing factor	Degree of automation		
	Manual	IP access solution	Process automation
Detection of FPGA-to-UUT topology	Manual analysis	Manual analysis	Automatic tool analysis
Provision of IP	Manual development	Use of predefined functional IP	Part of the system solution
IP mapping	Manual mapping	Pre-mapped IP	Pre-mapped IP

IP-to-pin configuration	Manual routing	Manual routing	Automatic routing
IP control	Completely manual scripting	Use of pre-defined access macros	Automatic scripting
Test data and guarding vector generation	Manual	Manual	Automatic test program generator
Creation of the overall project	Manual	Manual	Automatic
Diagnosis generation	Manual	Manual	Automatic diagnosis generator
Time for entire project creation	Several days to several weeks	Several days to several weeks	Minutes
Necessary FPGA design skills and FPGA development tools	Profound design knowledge and complete tool-chain	Profound design knowledge and complete tool-chain	none

Table 1: Characterization of various implementation strategies for FPGA-embedded instruments

With purely manual implementation, both the IP and the necessary process steps are carried out by the user. This requires extensive design knowledge about the target FPGA, as well as access to the complete tool-chain.
A strategy such as this can be very complex but requires minimal investment. A fully application-specific solution is ultimately produced.

Another variation is the use of preconditioned IP access solutions. In this variant, a sort of IP kit from a system provider is used. The IP includes the pure instrument function and also the JTAG mapping. Also included are predefined access routines such as read and write procedures, e.g. Based on Tcl (Test Command Language). Using such commercially available solutions shortens the project development time. They also offer the charm of relatively manageable investments, although the licence costs for an IP can be really quite high. This is associated among other things with a volume license, which is often required. However, many process steps must be carried out manually in this variant.

The third category is a complete system solution based on a framework with continuous process automation, such as ChipVORX® [3] by GÖPEL electronic represents. Here, analysers, configuration tools and generators do virtually all the work of the design engineer and test engineer. This procedure is based on the board's CAD data and an IP library. The IP is adapted to the target without manual intervention. Automatic test generators and diagnosis processors complete the system solution. The time it takes to create the project is typically a matter of minutes and the user does not need any special FPGA tools or design experience. As a result of the integration of ChipVORX into the system

platform SYSTEM CASCON [4], it is also possible to mix FPGA-embedded instruments applications with other embedded board test procedures such as boundary scan, or processor emulation, without any problems.
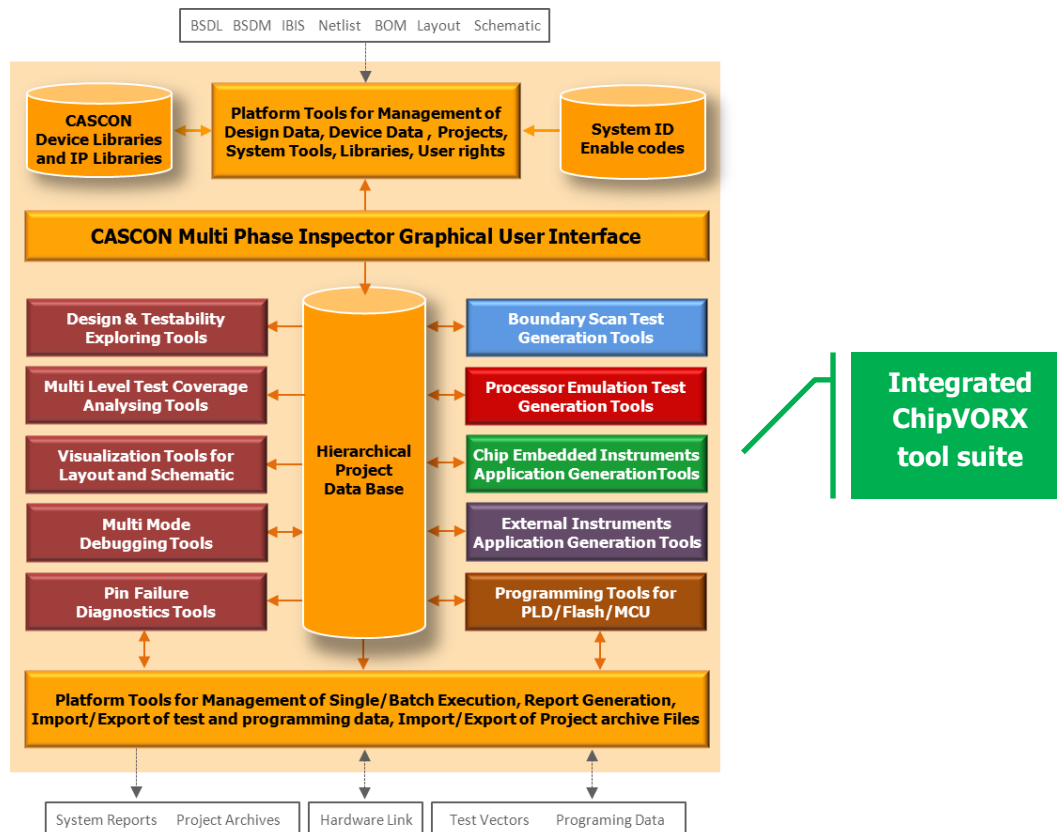

Figure 4: Architecture of SYSTEM CASCON with integrated embedded instruments tool suite

The joy of testing and programming

Thanks to the level of automation of FPGA-embedded instruments now available for board testing, recent years have seen a sharp increase in interest and the number of applications. According to Table 2, this is not just down to greater test coverage but also faster flash programming and improved options for validating embedded systems where physical access is no longer possible.

Focus of application	Objective	Comment
High speed flash in-system programming	Programming of serial flash (SPI, I2C), FPGA boot-flash, parallel flash (NOR, NAND)	Up to 100 times faster than e.g. boundary scan

RAM test	Test of the connections between FPGA and RAM (sRAM, dRAM…)	Higher test speed than boundary scan, but same pin-level diagnosis
Frequency measurement	Checking of clock signals (single-ended, differential)	Instrument can also be used for toggle detection
LAN test	Test of the connections between FPGA and external MAC/PHY	Protocol-based function test
Bit Error Rate Test (BERT)	Test of gigabit connections, incl. eye diagram visualisation	Support for parallel transmission channels such as e.g. PCIe x16

Table 2: Examples of ChipVORX applications

The gain in test coverage is achieved in particular due to the higher speed of the instruments. This enables problems to be solved, such as the problems experience with boundary scanning as a result of the low vector repetition rate. This is particularly relevant for flash programming due to the increasingly vast volumes of data, but also for testing of new DDR-RAM types, because certain dynamic minimum requirements must be complied with here. FPGA-embedded instruments are therefore a perfect complement to the embedded Board Test via Boundary Scan.
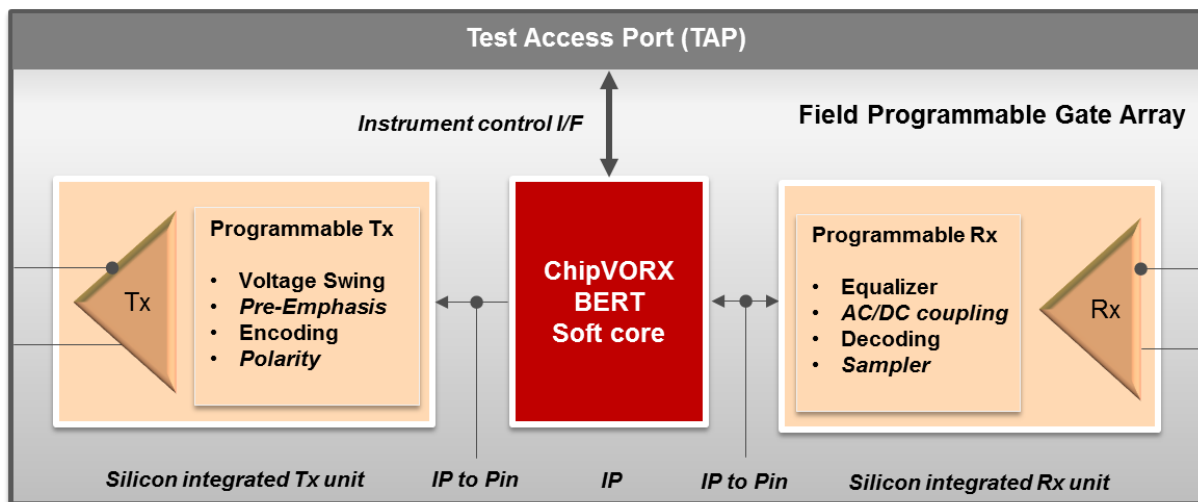

Figure 5: Typical architecture of a BERT-IP ChipVORX

The situation looks a slightly different when it comes to Bit Error Rate Tests (BERT) for GBit links, which can only be performed with a nominal operating speed, or under stress conditions. A purely numeric assessment of transmission quality is inadequate here, and eye diagrams are also required. In order to support such applications, the FPGA suppliers have permanently integrated sophisticated scanning mechanisms (so-called samplers) in the silicon, directly behind the GBit receiver. In this case, the

ChipVORX IPs also control these instruments, harmonised with the necessary interface parametrisation and the BERT pattern generators and analysers included in the IP (Figure 5). Since all the TX/Rx settings can be interactively adjusted, without new design synthesis, this also provides the design engineer with an effective means for link validation.

There are different modes for flexible flow control:

- Interactive debugging during project creation
- Interactive measured value visualisation with confirmation in run-time mode
- Standard run-time mode with numeric target/actual comparison of measured values
- Control of the overall process by parent entities (system integration)

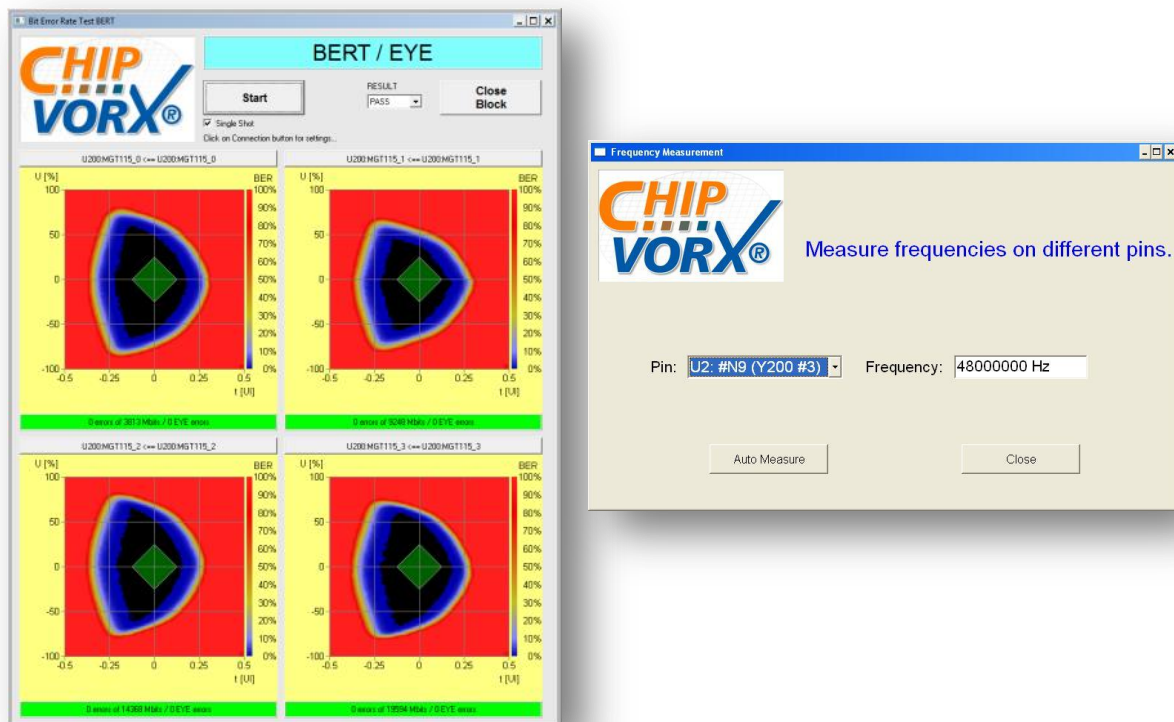Visualisation of measured values is in the form of panels (Figure 6).

Figure 6: Examples of ChipVORX visualisation: BERT-Eye (PCIe x4) and frequency measurement

The use of FPGA-embedded instruments with the concepts discussed above has not been discussed for a long time, however. Going beyond the principle of embedded test centres, FPGAs are also exceptionally suited for designing flexible, external test hardware. One example of this is the ChipVORX module (Figure 7). The concept behind it is really simple. The modules are brought to the same description level as the board to be tested using mapping and then processed with it as a single unit

by the tools. All features and procedures therefore remain identical, even though it is an external additional electronics unit. Using corresponding assembly modules, standard interfaces such as PCIe, SATAe or USB3.0 can also be tested on this basis. For boundary scan purposes, all these modules also support IEEE1149. 1 and IEEE1149. 6 [5].

Figure 7: ChipVORX modules with integrated FPGA

These modules are controlled via the normal test access port, and multiple modules of the same type or a different type can also be cascaded. A test station such as this (Figure 8) can be easily configured and even supports testing of objects which have no on-board FPGA. In addition, such modules can also easily be installed in fixtures and control test points contacted using needles.
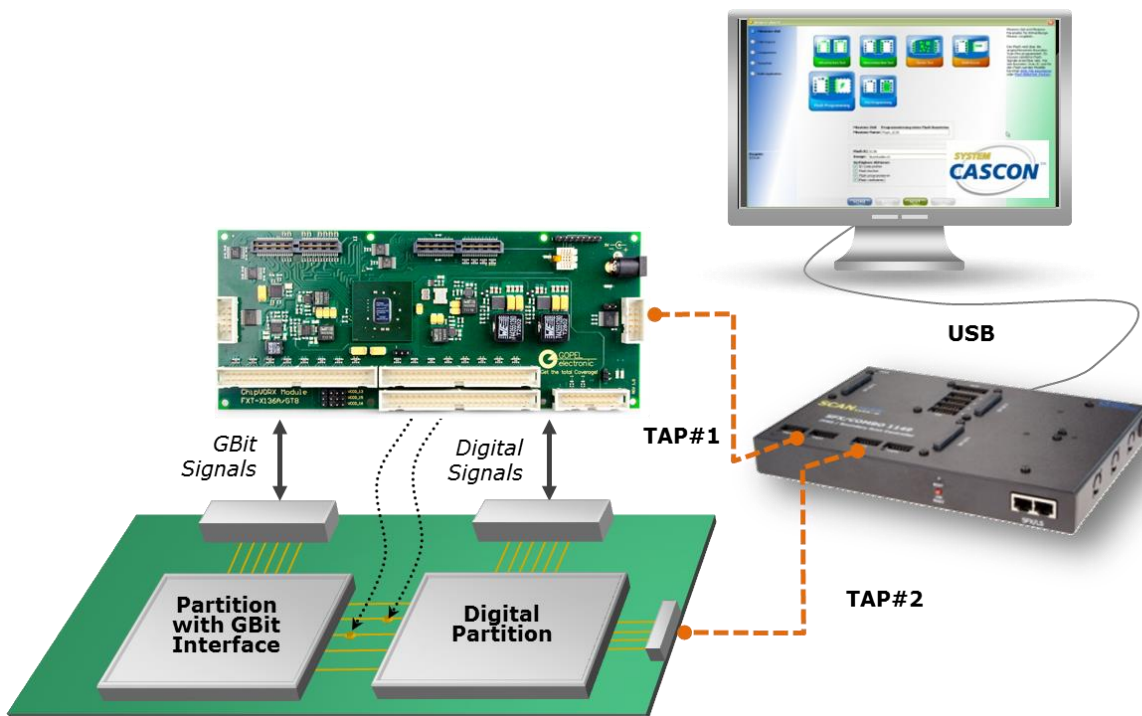

Figure 7: Complete test station with ChipVORX I/O modules

The ultimate in production testing can actually only be provided by a combination of all the embedded test procedures, such as Boundary Scan, Processor Emulation Test, In-System Programming and FPGA-embedded instruments in an environment that includes external I/O modules and other external standard instruments. Appropriately engineered hardware and software platforms such as SYSTEM CASCON are essential for this. This platform naturally also supports completely manual project development based on its own IP and convenient control at language level.

Summary and conclusions

As design-embedded test centres, FPGA-embedded instruments offer huge potential for improving the quality of testing and fault coverage for highly complex electronic systems with greatly reduced physical test access.
Constant innovations in FPGA are securing the future of such approaches for embedded testing in the long term. A great deal has also been done in recent years on the side of device technology. Users can select from a diversified number of approaches to suit their own individual requirements. In particular, the almost completely automated system solutions ensure incredibly short lead times and free users from the obstacles of specific FPGA knowledge and corresponding development tools. These are very important decision-making criteria, especially for EMS service providers.
The range of applications for FPGA-embedded instruments is virtually without limit. Even for GBit links, highly sophisticated tools now exist, and the portfolio of IP products is constantly expanding. External FPGA modules also offer the option of additionally improving testability on using native methods. If all these advantages are mixed with other embedded test strategies on a single platform, nothing can stand in the way of enjoying the board test made by FPGA.

References

[1] IEEE Std.1149.1-2013, Standard Test Access Port and Boundary Scan Architecture
[2]   IEEE Std. 1687, standard for Access and Control of Instrumentation Embedded within a Semiconductor Device.
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     Networks

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