Big test strategies in small packages

New applications such as the Internet of Things (IoT), networking in the automotive sector and Smart City, to name just a few, not only stimulate the development of innovative design technologies at the chip and board level, but they also permanently alter the electrical characteristics of modern electronics. This fact also has a fundamental impact on quality assurance methods in production. In particular, the question of the correct electrical test strategy and how to implement it technically repeatedly finds itself in the spotlight. The article below discusses a few fundamental issues relating to this and presents an innovative Tester on Chip (Toc), as well as its practical applications as part of a system solution.

Spoilt for choice

The fact that electronics need to be tested somehow at some point before delivery is surely undisputed. However, opinions and discussions on this topic differ greatly. While some argue that switching a product on and seeing if it starts is completely sufficient, others demand full testing, preferably at every stage in production.

Now there are actually applications where such practices are justified, for example the essential 100% testing coverage for components in the aerospace industry on the one hand or the simple mass-produced dimmer switch on the other.

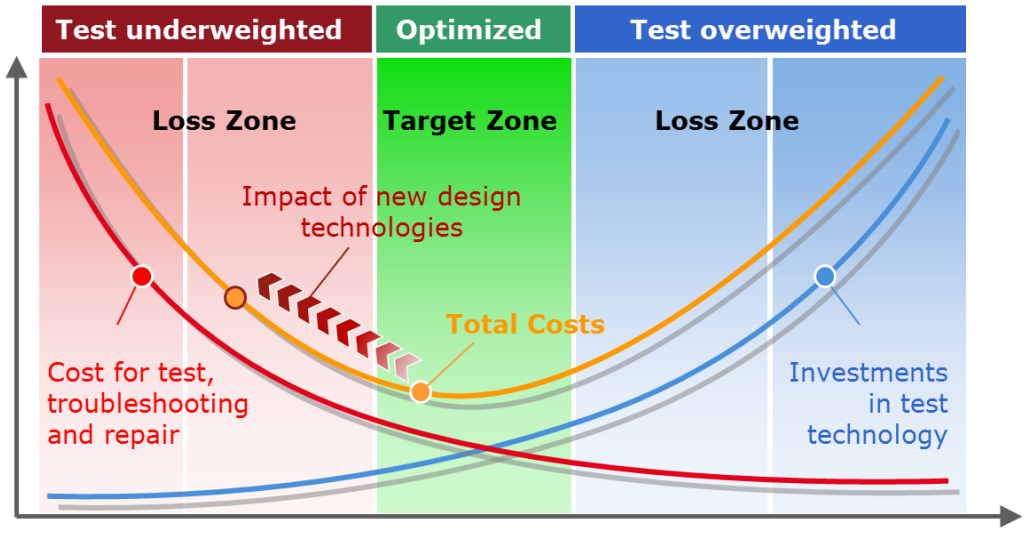

Figure 1: Qualitative cost trends for testing

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However, the cost relationship shown in Figure 1 applies in principle for the majority of complex electronic devices. Consequently, testing always also involves the problem of optimising costs and benefits. Too much testing results in unnecessary additional costs in the same way as too little testing. It is precisely on this point that opinions differ. Many things become intermingled in the discussion about the right level of testing, and it often ultimately comes down to which is the better tester. However, this tunnel vision automatically leads to decisions which are less than perfect, because it does not follow a holistic approach towards optimising costs throughout the product life cycle.

A more precise analysis of all the faults to be recorded at the end of production results in classification according to Table 1.

Fault category	Sources of faults (extract)	Primary UUT impact
Faults occurring during process operation (process faults)	- Paste printing - Assembly - Soldering - Installation	- Change in the electrical structure
Faults due to introducing defective or incorrect components into the process (introduced fault)	- Incorrect/defective bare boards - Incorrect/defective IC - Incorrect/defective passive components	- Change in the electrical structure or - Change in the functional behaviour
Faults arising due to incorrect or insufficiently validated design (introduced fault)	- Timing problems - Signal level problems - Thermal problems (drift) - Tolerance problems - EMC problems	- Permanent or temporary change in the functional behaviour
Faults resulting from incorrect, inconsistent, outdated firmware (introduced fault)	- Incorrect image in the FPGA Boot PROM - Incorrect image in the microcontroller - Incorrect image in the flash memory	- Permanent or temporary change in the functional behaviour

Table 1: Overview of typical fault categories throughout the production process

Component, design and software faults introduced in the production process in particular are a very bad issue, because it is precisely these which in some cases cause malfunctions that are difficult to diagnose and in extreme cases even cause sporadic outages, which first occur under very specific conditions in the End of Line (EOL) test, or even after delivery. Avoiding these faults must be right at the very top on the scale of quality assurance measures since combating these faults can help to save enormous costs. This approach also has a fundamental influence on the necessary testing and inspection strategies because, if it is

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possible to minimise the number of introduced faults, then the spectrum of faults primarily to be covered inevitably also changes. The focus is then on the identification of structural faults behind each process step, while malfunctions are in principle still only addressed in the EOL test.

A methodology with this structure for monitoring the process inputs, all process operations and the output is shown in Figure 2. It also enables the feedback of obtained testing and inspection information in the context of SPC monitoring [1].

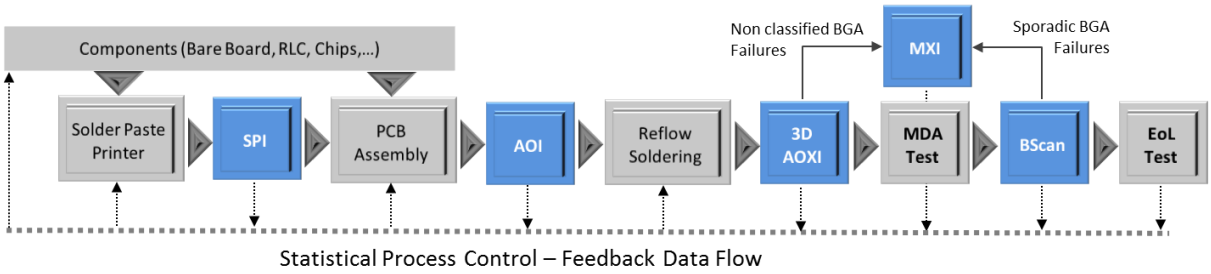

Figure 2: Example of a production line with SPC monitoring based on various sensors

On the basis of the documented philosophy, the test equipment used before the EOL test can focus on the diagnosis of the primary process faults. Depending on the available access methods, this results in the following methods:

- In-circuit test/manufacturing defects analyser based on invasive needle access
- Boundary scan test/IEEE1149.x on the basis of embedded system access (non-invasive)
- Function test via the native connector-access (non-invasive)

The test speed may well be in the static or at-speed range. The accuracy of the analogue function test need not be too great either, and plausibility tests are often sufficient.

The increasingly limited physical access to the unit under test (UUT) is the biggest obstacle to testing in modern assemblies, however. Technologies that have been tried and tested for decades, such as ICT/MDA, are therefore no longer widely applicable. In the digital domain, the JTAG/boundary scan access [2] has become increasingly prevalent here. However, here too, only a combination of various methods in one tester brings about the desired effect of maximising the fault coverage. Until now, the necessary instruments had to be combined in a discrete form, which was inevitably associated with higher integration complexity and costs. New problem-solving approaches are driving forward miniaturisation in this area significantly, however.

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Lots of music on the chip

Drawing on more than 20 years of experience, particularly in the area of boundary scanning and functional testing, GÖPEL electronic has developed the first mixed-signal Tester on Chip (ToC) that can be controlled via JTAG: the CION-LX [3]. It is characterised by the following main features:

- 32 mixed-signal channels, 8 differential channels, 4 high-current channels
- Support for IEEE1149.1, IEEE1149.6 and IEEE1149.8.1
- Integrated analogue resources (ADC, DAC, digitiser, Arb)
- Analogue front-end multiplexer
- Integrated digital resources (frequency counter, event detector)
- Switchable pull-up/pull-down
- Programmable slew rate for digital drivers
- Vio range of between 0.9 and 3.6 V on 4 different banks
- 3 different operating modes

The block diagram of the CION-LX (Figure 3) provides an overview of the overall architecture of the chip. It is manufactured using mixed-signal CMOS technology and is integrated in an LGA116 package.

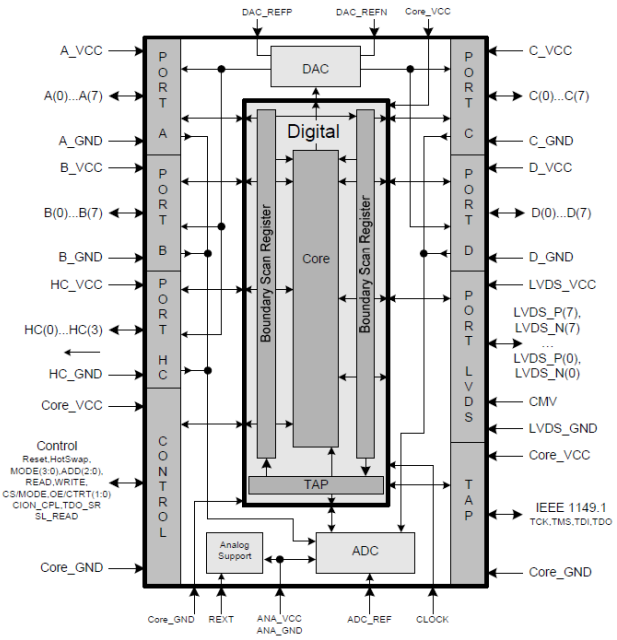

Figure 3: Architecture of the CION-LX

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In order to control the individual resources via JTAG, the chip has an extended register architecture with a total of 7 data registers and a 5-bit instruction register (Figure 4). Of these, 3 registers are used exclusively to manage the additional resources. The maximum TCK frequency is 100 MHz.

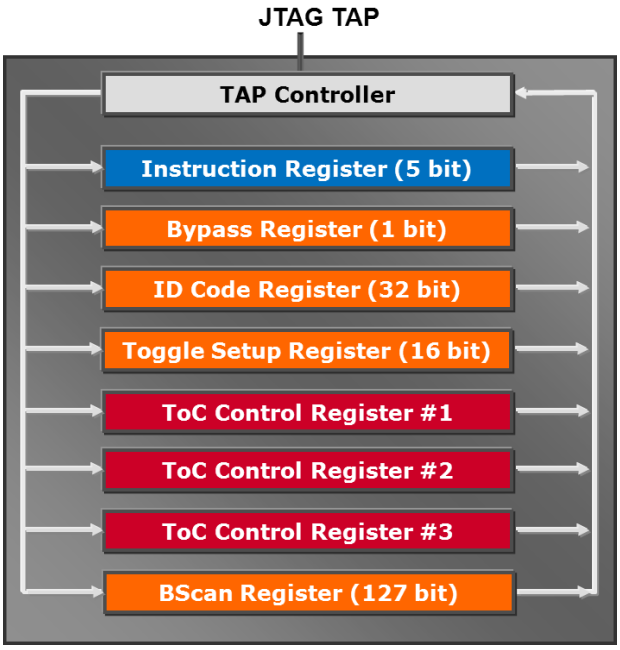

Figure 4: Test Access Port (TAP) organisation

Each of the 32 single-ended channels offers the option both to perform boundary scan operations and to use mixed-signal resources (Figure 5). A 2-bit boundary-scan cell architecture with bidirectional properties is used here. As a result, each channel can be independently characterized switched as input, output or tri-state (hot-swap). If desired, the additional instruments can also be used in parallel with the digital boundary scan I/O operations.

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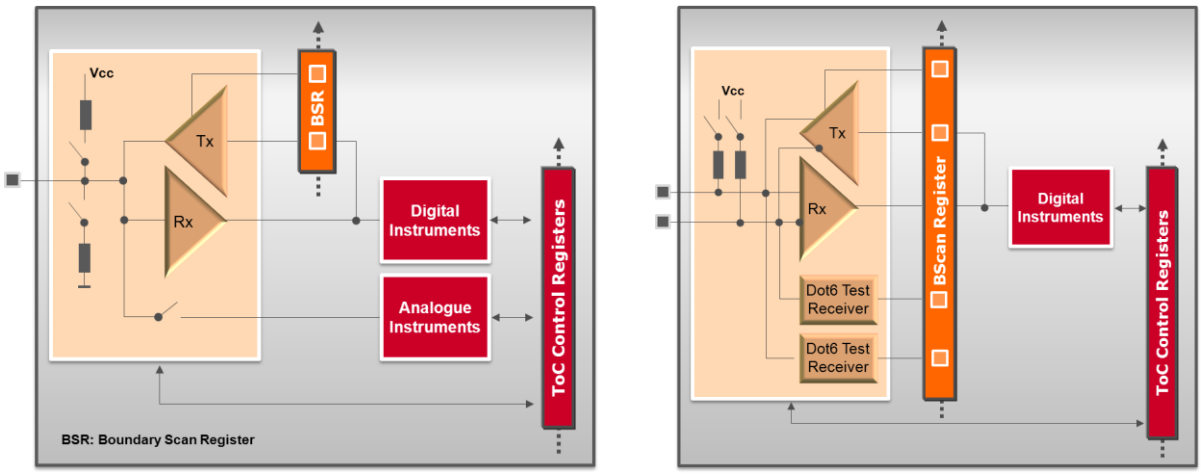

Figure 5: Structure of a single-ended channel and of a differential channel

In addition to the single-ended channels, the CION-LX also has integrated in it 8 bidirectional, differential channels with IEEE1149.6 [3] support. Only the digital supplementary instruments can be used with these (Figure 6). The boundary-scan cell architecture here consists of 4 bits.

To improve flexibility, the interface can be programmed in various parameters such as bias and scheduling and can optionally be programmed to CML or LVDS.

As already documented in Figure 3, the ToC also has a core logic. Depending on the selected operating mode, this includes either a 16-bit register or multiple buffer stages. This transforms the module into a parallel bus module. Both the boundary scan structures and the mixed-signal resources are used in this case too, but access in these modes can then also be in parallel and at a higher speed. The universality and thus the application bandwidth is significantly increased as a result.

Applications in a nutshell

With the properties already shown and the additional operating modes, there are many conceivable application scenarios for the CION-LX. These include

- Use as a purely serially controlled JTAG chip on an external test adapter
- Use as a simple 16-bit bus register with extended boundary scan testability
- Use as a double-clocked 16-bit bus register with extended boundary scan testability
- Use as an 8-channel driver/sensor interface for ATE pin electronics
- Use as a 16-bit level shifter with extended boundary scan testability

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- Use as a design-integrated system monitor with JTAG interface

In principle, any number of ToCs can be connected to extend the number of channels. In serial JTAG operation this is done by simple cascading, in parallel mode by addressing.

In addition to the individual chip, there are also a few pre-assembled I/O modules already available.

This also includes an evaluation board (Figure 6). It enables verification of all the features and operation modes of the CION-LX. Additional LEDs and an integrated clock module provide additional support.

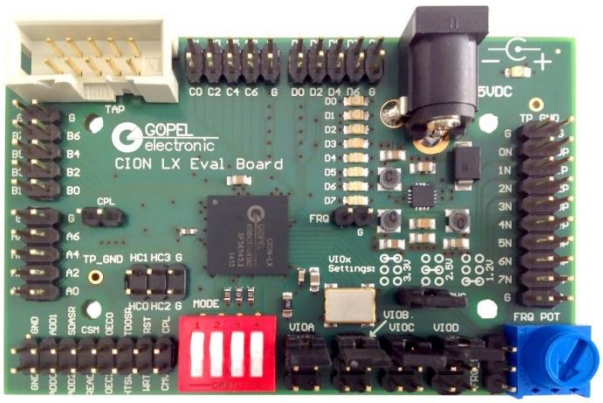

Figure 6: The CION-LX evaluation board

The CION-LX I/O module FXT/96 is available for use on an external test adapter. It has 96 mixed-signal test channels and is controlled purely via the TAP interface. It can be operated using any IEEE1149.x compatible controller.

Figure 7: The CION-LX module FXT/96

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First use of the CION-LX in parallel mode was recently introduced to the JTAG/boundary scan hardware platform SCANFLEX in the context of a new I/O module (Figure 8). The SFX5296LX has 96 single-ended mixed-signal channels and can also perform IEEE1149.x operations. It is controlled in parallel via the internal SCANFLEX bus and is therefore much faster than the CION-LX module FXT/96, for example, when it comes to performing test and measurement functions.

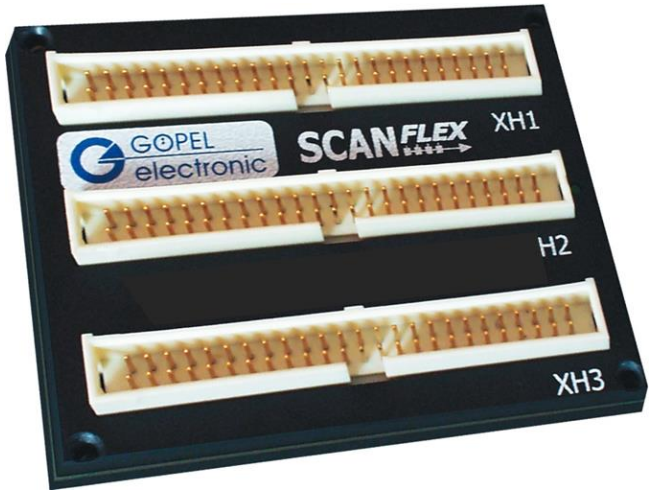

Figure 8: The SCANFLEX mixed-signal I/O module SFX5296LX

All modules previously shown are fully supported by the JTAG/boundary software platform SYSTEM CASCON™ [5]. Combined with a simple, low-cost controller such as the PicoTAP ™ and a CION-LX module FXT/96, it is already possible to configure a powerful mixed-signal test system.

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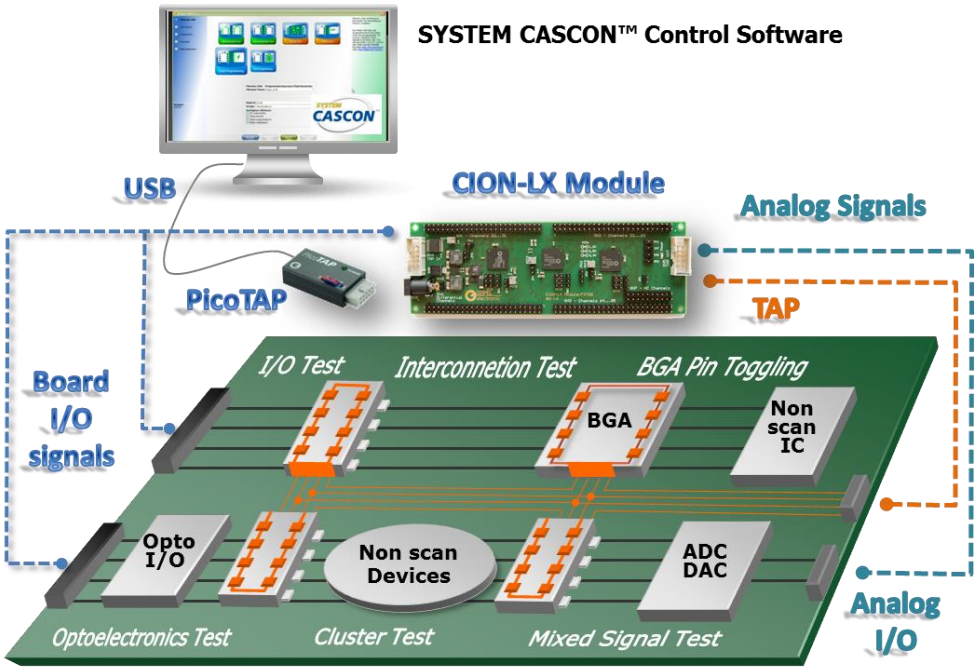

Figure 9: Example of an extended mixed-signal tester based on CION-LX

There is a multitude of procedures that can be performed, ranging from static digital patterns to at-speed analogue signals. We then get the following broad overview:

- Static IEEE1149.1 boundary scan tests for single-ended I/O
- At-speed tests via IEEE1149.6 for differential I/O
- Selective pin toggling based on IEEE1149.8.1
- Static digital function test
- Operation of digital levels with various slew rates
- Connection of pull-up/pull-down
- Frequency measurement
- Identification of random signal changes
- Generation of pulses/clock pulses
- Measurement of static voltages
- Digitisation of analogue signal curves
- Synchronised sampling of multiple analogue signals
- Generation of static voltages
- Generation of arbitrary signals
- Flash programming with possible external access

The resolution of the analogue resources is 12 bit for the ADC and 10 bit for the DAC. Although an internal reference voltage is integrated for the analogue resources, it can also

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be fed in externally. In addition, operation of the ToC merely requires an external clock generator.

In principle, all of the listed functions are available on all channels (with the exception of the differential channels) and some can also run in parallel, controlled autonomously in the chip. This flexibility makes the desired high fault coverage possible.

Taken as a whole, the CION-LX thus reinforces the philosophy of so-called Embedded System Access (ESA) developed by GÖPEL electronic [6].

Summary and conclusions

Modern electronic devices are becoming ever more complex, smart and fast and physical access is increasingly declining. These trends also have a strong impact on the resulting testing costs. In order to optimise costs and benefits, holistic optimisation strategies are necessary here which consistently minimise faults, particularly those introduced in the production process. Under these conditions, the test strategies used and the equipment necessary can focus primarily on the diagnosis of pure process faults. Driven by the reduced possibilities of physical contact, lying at the heart of this are instrumentations which utilise access mechanisms that are embedded in the system (e.g. JTAG/boundary scan) or the native connector-access (mixed-signal function test). New developments in the area of Testers on Chip (ToC), such as the CION-LX, enable the combination of such methods miniaturised in an IC. Various operating modes additionally enhance the universality of the chips. This provides an excellent basis for cost-effective implementation of highly integrated test solutions with excellent fault coverage.

The challenge of providing big test strategies in small packages is thus met, but the necessary boundary conditions must also be created on the process side in order to ensure success.

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