Thomas Wenzel

Test & Measurement Technology goes Embedded

The Electronics World speaks Embedded

No doubt! The term "embedded" is omnipresent and can be found in nearly every development sector. And everybody is busy to broaden the "embedded" factor – be it on the chip level or on the board level. Particularly the high rate of innovation found at microcontrollers and FPGAs widely opens up the door into an all new world of opportunities to create multi-functional electronics, which is best described to be more intelligent, more suitable for networking, re-configurable and compact-sized. New 3D chip technologies will boost this trend even further as the hunger for smart solutions in sectors like cars, consumer electronics, aerospace and industrial electronics is nearly unappeasable.

Successful development of such highly complex products not only requires excellent command of software design, FPGA design and board design. No less important are excellent skills in coordination of all distinct stages of development – from design concept via design and implementation to final prototype validation. In this context the so-called "V-model" plays an important role (figure 1).

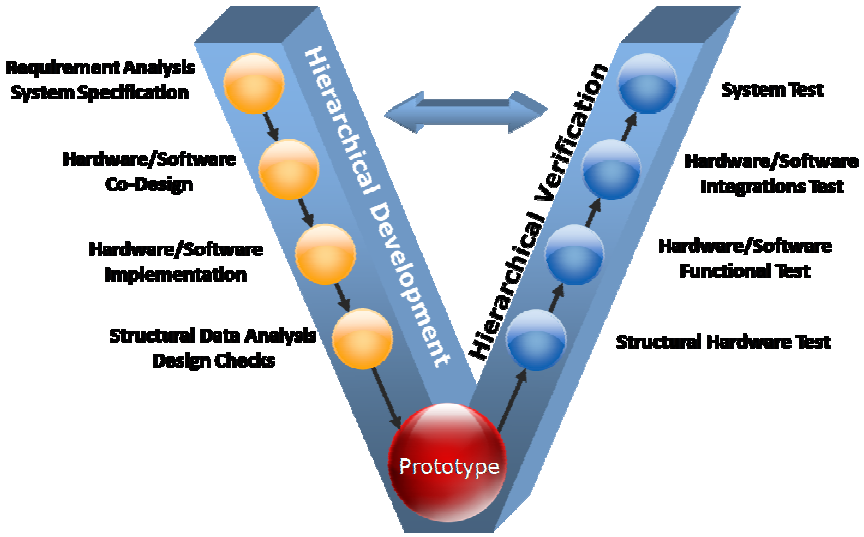

Figure 1 – Definition of hierarchically structured development and verification

The V-model defines adequate verification procedures for every design step to ensure a structured final overall validation. Throughout the current model, structured process steps have complemented pure functional considerations. This is due to the fact that structured validation and tests as

elements of a design-for-testability strategy have become standard in modern design and production test environments and their importance is even rising.
To be able to meet the requirements of hierarchical validation designers are equipped with a constantly widening and highly performant spectrum of instruments like, e.g. emulators, scopes, logic analysers, bit error rate testers (BERT) and many more. So the developers' world should look great. Really? Let's dig a bit deeper.

The Crucial Task of Getting the Signals

When discussing the situation of verification with designers and test engineers, one phrase obviously dominates the scene: accessing signals. In the good old days almost every pin or at least every net was available to be contacted for verification or test. The ever-increasing use of fine pitch components, BGAs and buried conductor traces turned this into a real nightmare. The discrepancy between the required size of test points and ever shrinking feature size gets worse day by day.

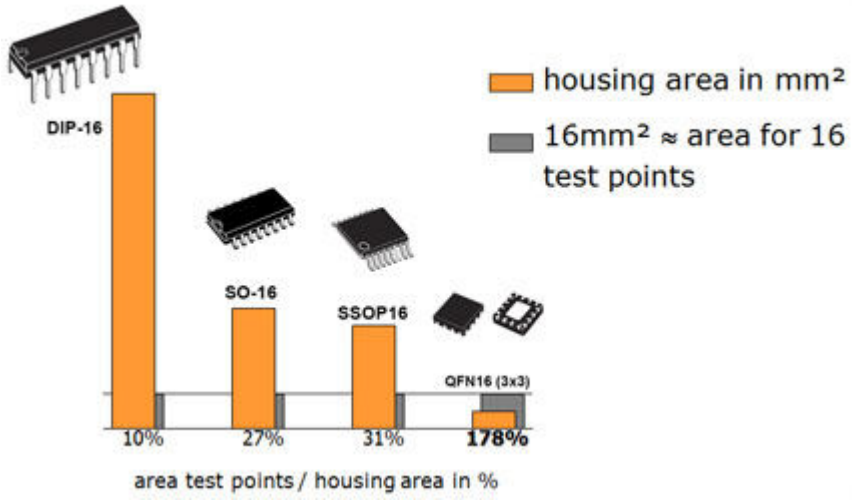

Figure 2 – The required board area for test points is getting more and more critical

The classic strategy of in-circuit-test probing of signals today can only partly serve as a developer's means of accessing the required signal information. The tactile access to the object to be verified is more and more reduced to access via native connectors. Test engineers suffer from the same experience when it comes to the use of the traditional in-circuit-test strategies in production. Here the same already mentioned trend of miniaturisation in electronics leads to problems: reduced test coverage, tremendously increased costs of faultfinding and finally the feared no-failure-found syndrome. The common suffering, however, sometimes leads to completely different reactions. Some people start to haggle over every test point for every new design, others seek their salvation in using flying probe testers, which are capable of contacting very small areas down to pin lands and still others claim to improved functional tests as the only way out. However, there is a big "but" for designers, as neither in-circuit-tests nor flying probers can really help to solve the validation problem. And test points are a dying species. So the need for an alternate strategy is really urgent here. But if access is possible, all this discussion should no longer be any topic, should it?

The Art of Meaningful Seeing

To transmit and process information faster and faster you need to increase the speed of internal signal flow. There's no way out. In addition to the transition to parallel processing using multi-core systems, an increased signal transmission rate is on the focus of designers. Especially the changeover to serial Gigabit links manifests itself as a number one topic. Externally, such Gigabit connections are implemented using standard communication buses like, e.g. USB3.0, PCI Express or SATA Express. But also board-internal they are increasingly used as high-speed transmission medium for chip-to-chip communication. One of the top drivers of innovation is FPGA technology. The latest generations of FPGA devices from Xilinx or Altera offer fantastic transmission rates of up to 28 Gbit/s – in parallel on up to 96 channels.

However, the design-in process of such Gigabit links requires great care. This isn't surprising at all. Due to the high frequencies involved, these connections are more and more bound to the typical challenges of analogue technology, though differential transmission technology takes out some of the heat. Anyway, the design rules are extremely stringent and require an impedance-matched implementation to ensure the highest quality of signal transmission. High-quality Gigabit analysers with special test probes are available to validate such connections. Nevertheless, probing of Gbit signals will always affect signal integrity. It's like the task of touching a glassy water surface without generating waves. No chance, waves could be minimised at the best. Modern Gigabit analysers try to tackle this problem using some sort of de-emphasis to compensate for probe properties. The really induced anomalies, however, can only be precisely calculated, when the interaction of electrical properties of probe and probe target are known – and thus they remain invisible. The transmission frequency is the key figure in this context and as it is ever increasing, anomalies will be increasing too; so external instruments will hit their natural limitation (figure 3).

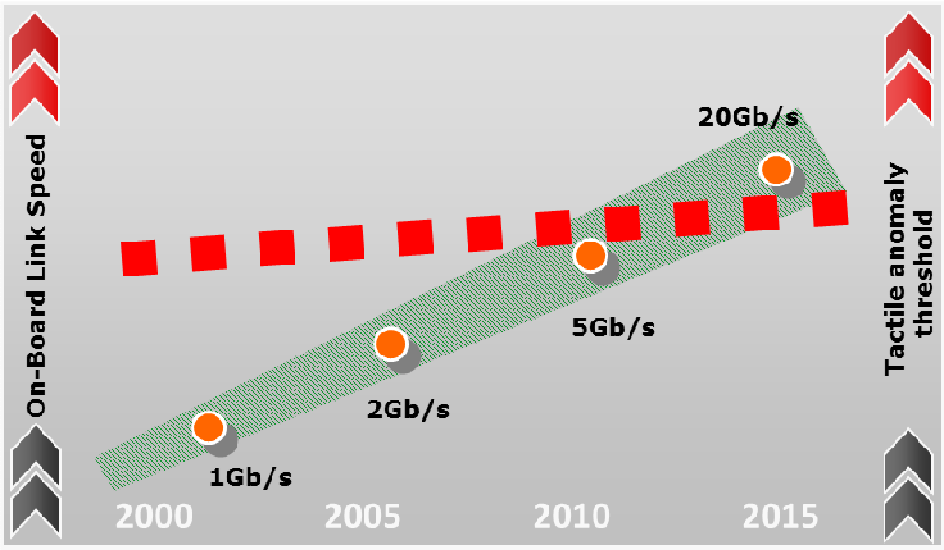

Figure 3 – Probing of Gigabit signals hits a critical limit

Assessing the whole picture from the design's point of view clearly spells out: we don't see what silicon sees. And this becomes increasingly problematic.

The Move to Embedded System Access (ESA)

Analysis of current access strategies suggests a division into three classes:

- Native Connector Access (test access via design relevant I/O signals)
- Intrusive Board Access (artificial access via test nails and probes)
- Embedded System Access (natural test access via design-integrated test bus)

In practice, these classes are not isolated but can be applied in common.

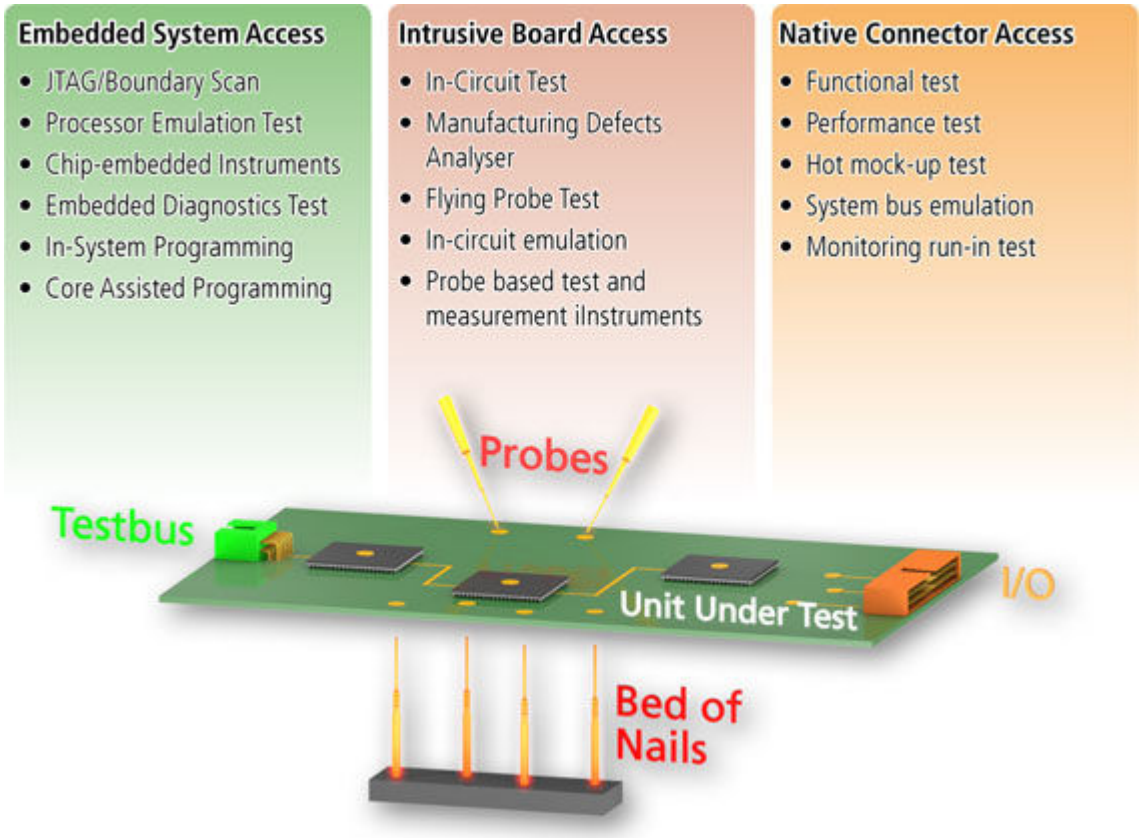

Figure 4 – Classification of the strategy of electrical access at board level

Within the light of the above outlined problems the so-called Embedded System Access [1] sounds promising. The roots are reaching back more than twenty years – originating from the boundary scan test method, which has been standardised in 1990 as IEEE1149.1 [2]. Driven by evolutionary developments ESA today covers a variety of non-intrusive technologies to validate, test, debug and programme electronics assemblies. These include in particular:

- Boundary Scan Test (IEEE1149.1/4/6/7)
- Processor Emulation Test (PET)
- Chip Embedded Instrumentation (IJTAG/IEEEP1687)

The basic idea of ESA is, to replace the tactile access by an access, which is integrated into silicon. In principle, every ESA technology has its task-specific "pin driver" electronics, which is controlled via a test bus to run test functions or programming tasks directly in-system. The target system may be a chip, a board or an entire unit; hence it is totally independent of the hierarchical application

level. So the Embedded System Access concept can be used throughout the V-model and the entire product life cycle.

Test & Measurement Technology gets System-Integrated

The transition to Embedded System Access isn't just a small adaptation of how to handle test and programming vectors: it is a paradigm shift. The practical use of the Embedded System Access implies the conversion of a UUT's pure functional design into a tester-UUT-configuration (figure 5).

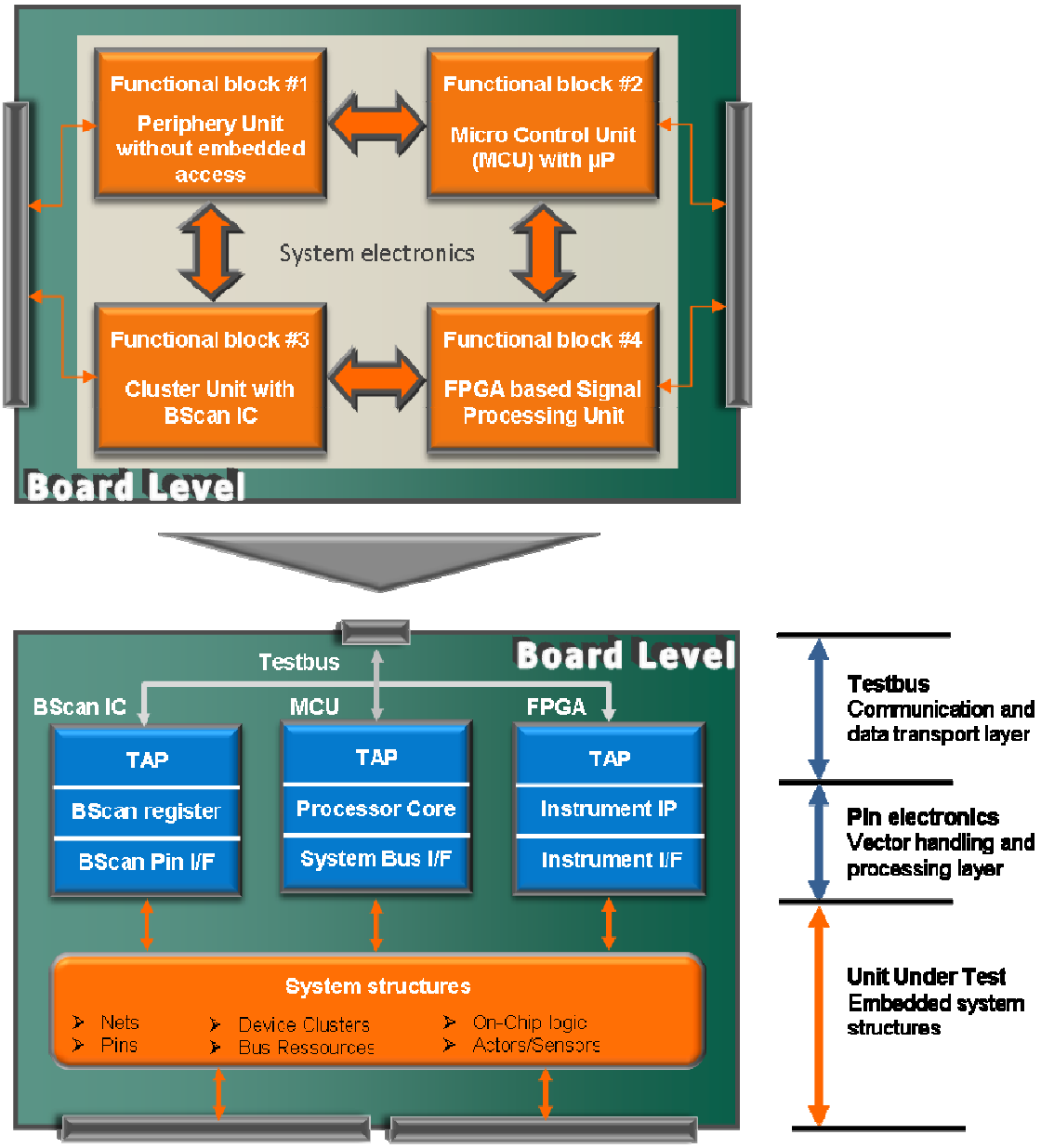

Figure 5 – Principle of transformation for use of Embedded System Access

The transformation forms a three level infrastructure. This infrastructure is comprised of a test bus (typically JTAG) as control medium, the so-called pin electronics, which provides the internal interface to the target and the elements of the unit under test that shall be validated or tested. The pin electronics is driven by boundary scan, the microprocessor and chip-embedded instruments. But

what, precisely, are chip-embedded instruments and how can they solve the problem of Gigabit links?

Instruments that really see the Silicon

Chip-embedded instruments are test and measurement intellectual property (IP) blocks integrated into ICs, which are controlled via the test bus (figure 6). Of course the IC may have additionally boundary scan included.

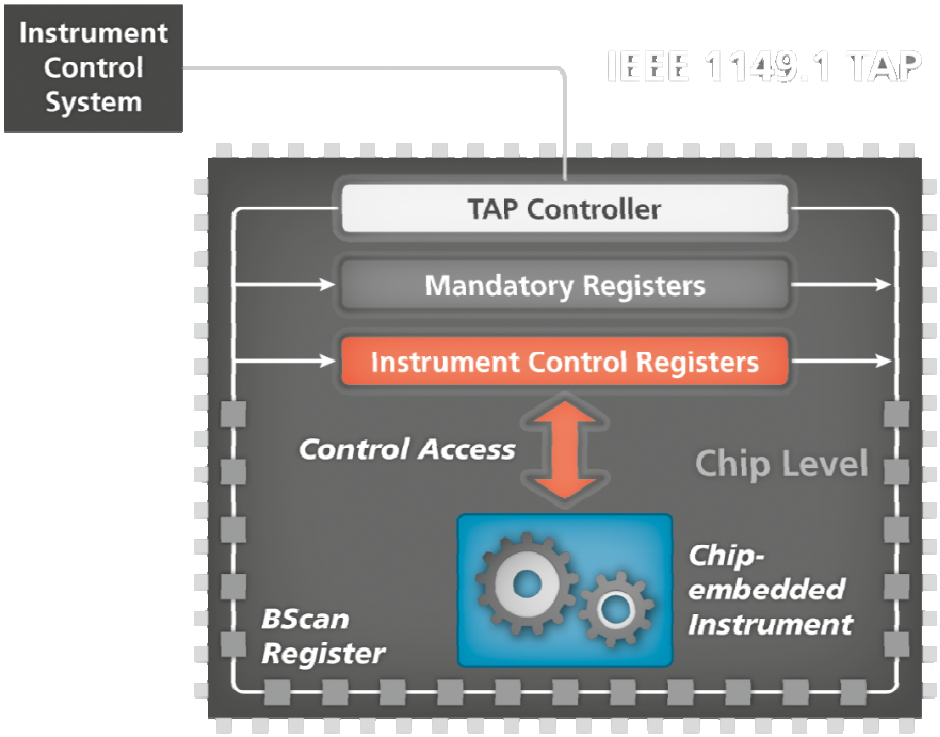

Figure 6 – Boundary scan IC includes chip-embedded instrument

Examples of chip-embedded instruments:

- Voltmeter
- Frequency counter
- Thermometer
- Bit-error-rate tester (BERT) for high speed signals
- Pulse counter
- Logic scope
- RAM tester
- Built-in self-test circuitry
- In-system programmer

The IP is either permanently integrated in the chip (hard macro), or it can be temporarily instantiated and configured (soft macro) in Field Programmable Gate Arrays (FPGA). As all instruments can be controlled serially or in parallel, the user gets a comprehensive insight into the circuitry to be tested and will see, what the silicon sees. The JTAG test bus is used as transport

medium for data and control commands. This bus is connected with a JTAG controller, which in turn is controlled via the system software.

Figure 7 – Chip-embedded instruments pave the way for many applications

Basically, chip-embedded instruments are not a new invention as they have been utilized for years in chip test, for example in form of built-in self-test (BIST) IP. However, access to these instruments has not been standardised in the past, something that will be changed with the new standard IEEE P1687, which is currently under development (IJTAG) [5], or IEEE1149.1-2012 [6] (figure 8).

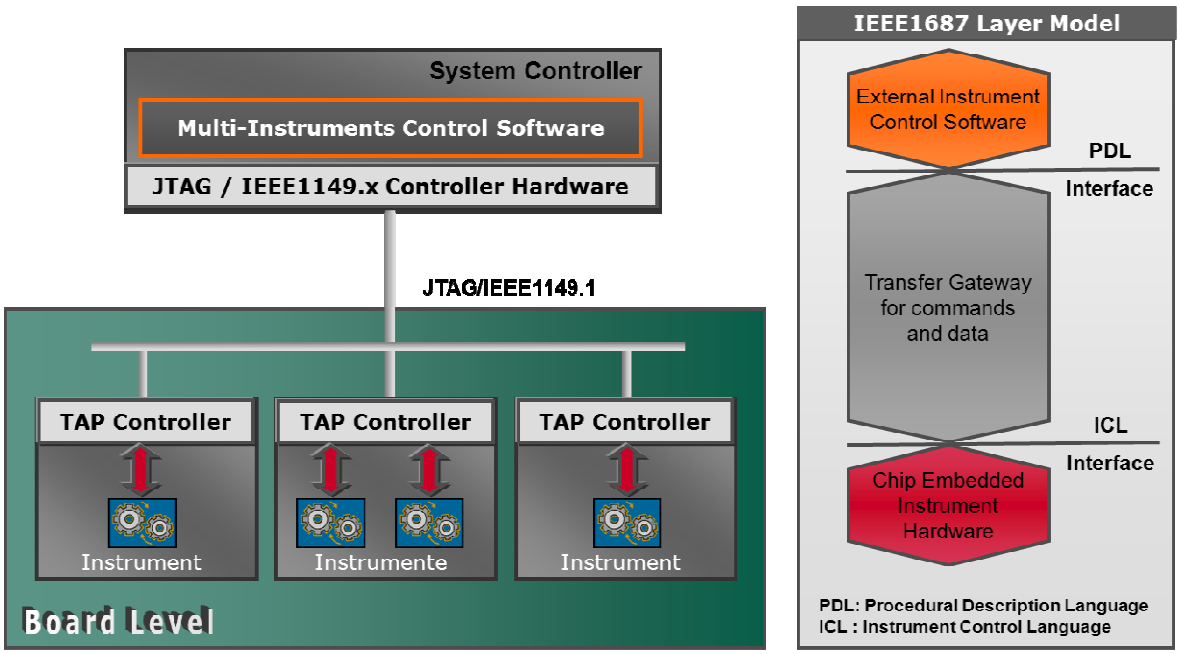

Figure 8 – Structured access to chip-embedded instruments according to IEEE P1687

Flexibility unlimited: FPGA Embedded instruments

In particular, FPGA Embedded instruments, based on soft cores, have enjoyed strong interest recently. By enabling strategies such as FPGA Assisted Test (FAT) and FPGA Assisted Programming (FAP) they provide an enormous flexibility for the adaptation to individual test and measurement requirements. The idea behind is rather simple. Based on the circuit and the measuring task, a corresponding IP will be uploaded into the target FPGA, configured, controlled and finally removed again after having finished the jobs. Various test systems do exist, which are capable to automate the handling of these processes. However, they differ in the way of IP generation. Basically it's all about how to join an existing IP to the corresponding signal pins (IP to Pin). Traditional systems therefore require an extra synthesis run, which can be time-consuming and inflexible during interactive debugging.

In contrast, the ChipVORX® technology [7] uses a special method, which doesn't require synthesis runs and can be adapted to new tasks in a fraction of a second (figure 9). It relies on the same project database and the same runtime system as boundary scan does.

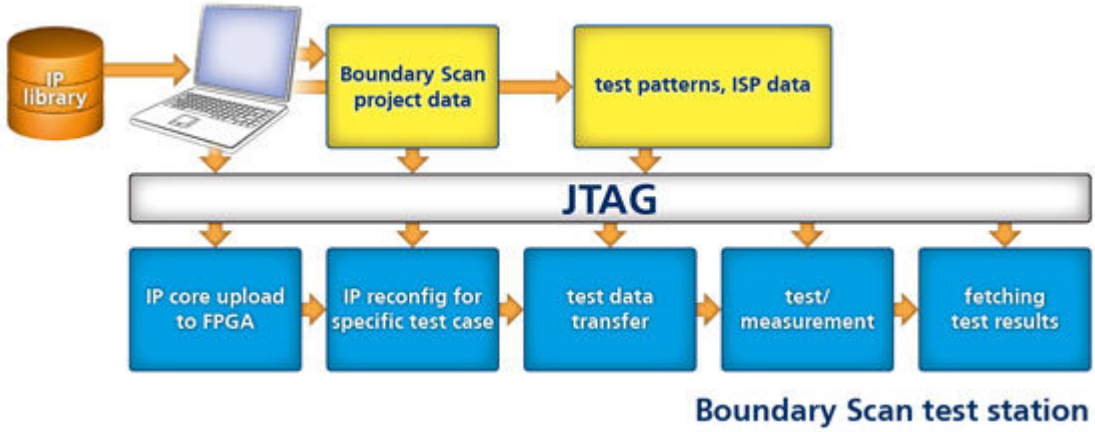

Figure 9 – ChipVORX uses automated IP handling

Moreover, ChipVORX comes with more than 300 preconfigured IPs and supports all common FPGA platforms for numerous applications like RAM access test, frequency counter, BERT or in-system programming of Flash memories. Compared with boundary scan, Flash programming runs up to 75 times faster and the RAM access test can reach a speed-up factor of 20. For debugging purposes appropriate panels are generated (figure 10).

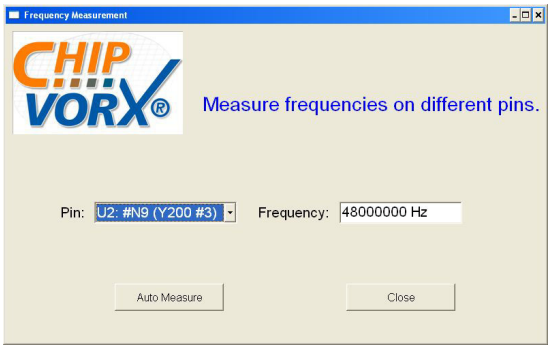

Figure 10 – Interactive ChipVORX panel for frequency measurement

New IPs are available to support bit error rate tests. Also these instruments don't require synthesis and can be used for design validation (figure 11) and production test, when included in a test programme.

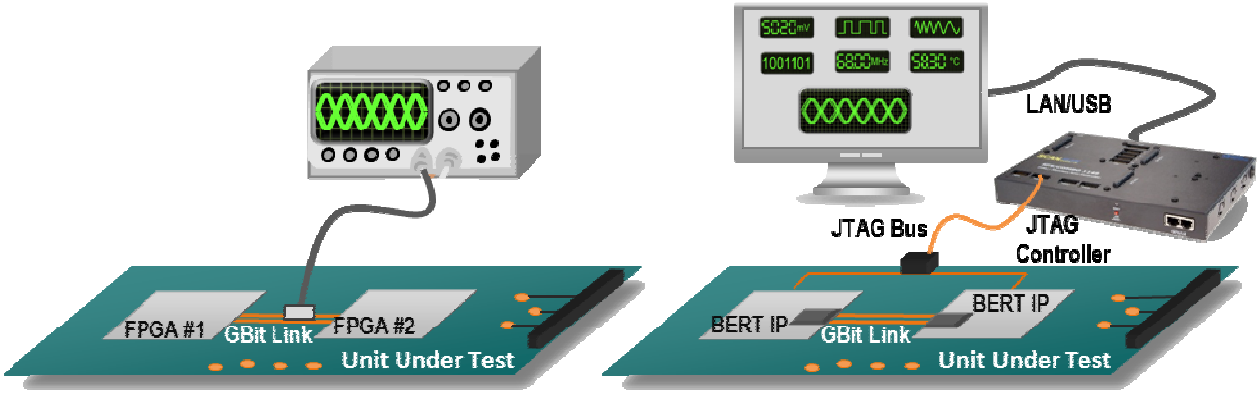

Figure 11 – BERT goes FPGA-embedded

During production test the bit error rate will be only checked for plausibility based on pre-defined setups, whereas during design validation even the eye pattern can be graphically visualised (figure 12).

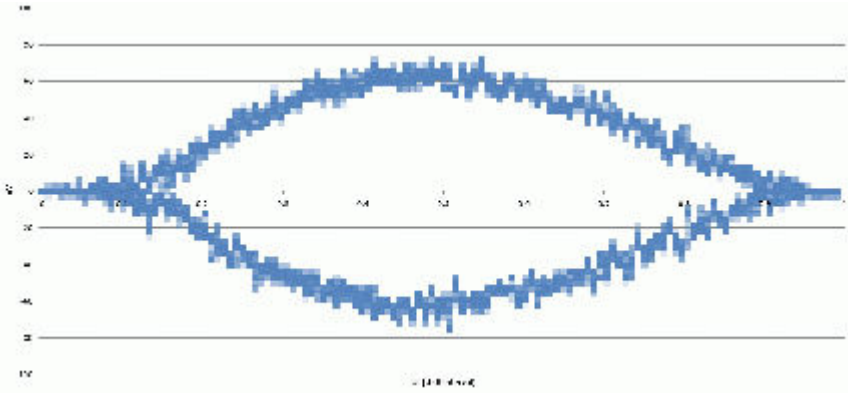

Figure 12 – Visualisation of the eye pattern during FPGA Gbit link validation

This kind of visualisation is carried out directly in silicon and thus avoids the anomalies caused by tactile probing.

Summary and Outlook

The transition towards Embedded System Access has initiated a real paradigm shift regarding validation, test, programming and debugging of complex electronics units. Within this context, more and more instruments are directly implemented in silicon or uploaded into FPGAs as soft macro to be able to see exactly what silicon sees. New standards drive standardised access to these instruments and facilitate their use throughout the entire product life cycle. In perspective, particularly FPGA-embedded instruments are promising an enormous applicability. However, test systems must be capable of efficiently putting these possibilities into practise. In this respect it is of paramount importance that these innovative test and programming strategies can be run both stand alone and in combination with intrusive test access methods like in-circuit-test on a common platform.

For additional information, you can contact the authors, Thomas Wenzel and Stefan Meissner, per e-mail under t.wenzel@goepel.com and s.meissner@goepel.com.

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